



User's Manual

3312390

---

**Copyright © 2003**

**All Rights Reserved.**

**Manual edition : 1.0 March 2003**

The information in this document is subject to change without prior notice in order to improve the reliability, design and function. It does not represent a commitment on the part of the manufacturer.

Under no circumstances will the manufacturer be liable for any direct, indirect, special, incidental, or consequential damages arising from the use or inability to use the product or documentation, even if advised of the possibility of such damages.

This document contains proprietary information protected by copyright. All rights are reserved. No part of this manual may be reproduced by any mechanical, electronic, or other means in any form without prior written permission of the manufacturer.

#### **Trademarks**

PC is a registered trademark of International Business Machines Corporation. Intel is a registered trademark of Intel Corporation. AWARD is a registered trademark of Award Software International, Inc. DiskOnChip®2000 and TrueFFS are registered trademarks of M-Systems Inc.. Other product names mentioned herein are used for identification purposes only and may be trademarks and/or registered trademarks of their respective companies.

---

# Table of Contents

<b>Introduction .....</b>	<b>5</b>
<b>Specifications .....</b>	<b>6</b>
General Specifications .....	6
High Speed Multi I/O .....	6
Network Interface Controller .....	7
Display Controller .....	7
Environmental and Power .....	7
<b>Board Image .....</b>	<b>8</b>
Ordering Codes .....	9
<b>Board Layout Front .....</b>	<b>10</b>
<b>Board Layout View (Back) .....</b>	<b>10</b>
<b>Jumper/Connector Quick Reference .....</b>	<b>11</b>
<b>Watchdog Timer .....</b>	<b>12</b>
Timeout Values .....	12
Timeout Table .....	12
<b>Flat Panel VGA .....</b>	<b>15</b>
<b>System Resources .....</b>	<b>16</b>
<b>ETX Connector .....</b>	<b>18</b>
<b>ETX Connector .....</b>	<b>19</b>
<b>AWARD BIOS Setup .....</b>	<b>20</b>
Setup Items .....	21
Standard CMOS Setup .....	22
IDE Harddisk Setup (submenu) .....	24
BIOS Features Setup .....	26
Chipset Features Setup .....	29
Integrated Peripherals .....	34
Power Management Setup .....	37
PnP/PCI Configuration .....	39
PC Health Status .....	41
Frequency/Voltage Control .....	42
<b>POST Codes .....</b>	<b>43</b>
<b>Howto : Flash the BIOS .....</b>	<b>50</b>

---

What if things go wrong .....	51
<b>Warranty .....</b>	<b>52</b>

---

## Introduction

This ETX is based on Intel Celeron and PIII Tualatin ULV (Ultra Low Voltage) Technology with VIA chipset which combines PC-100/133MHz FSB, UltraDMA/100 IDE technologies and rich 4xAGP 2D/3D graphics capabilities in a single package. Its onboard single RTL10Base-T/100Base-TX Fast Ethernet, CRT /LCD display controller, with VGA / TTL / LVDS and TV-Out Interfaces add communication and multimedia features to its powerful function.

Arbor's ETX CPU Module provides a series of reliable and powerful ready-to-run computing platform with Intel processors range from Celeron and Pentium III Tualatin. This series is easy to upgrade for the customer's advanced CPU and application development needs. The ETX core is 95 x114mm that makes wide flexibility in carrier-board form factors. This carrier board can either be customer designed or done with Arbor's dedicated customization team. With the smart concept of providing a complete CPU system module that mounts onto an easily designed application carrier board, ETX products allow ODM embedded integrators to better focus on their intended application that can save 80% of regular development time and costs, plus speed up time to market.

The new Intel CPU ULV Tech. will spur the further development of the emerging new generation of quiet running, low profile small factor designs that are being adopted for a myriad of connected information and entertainment systems and provides more low power consumption - ranging from home entertainment devices such as Set Top Boxes, Game Consoles, Personal Video Recorders and Broadband Gateways to commercial applications such as Thin Clients, LCD Web Based Terminals, POS Terminals and Network Attached Servers.

With its Ultra Low Voltage, rich levels of integration, advanced multimedia capabilities and communication features, this board is an exciting opportunity for System Integrators and OEMs to develop new generation products that meet the desires and aspirations of the 21st century consumers.

---

## Specifications

### General Specifications

- **CPU** : Intel Ultra Low Voltage Embedded Celeron 400MHz to Pentium III 933MHz processor with FSB 100/133 MHz EBGA package.
- **Chipset** : VIA VT8606 TwisterT with Integrated Savage4 AGP 4X Graphics core and VT82C686B Super "South Bridge"
- **BIOS** : AWARD® Flash BIOS
- **Green Function** : power saving supported in BIOS. DOZE / STANDBY / SUSPEND modes, ACPI & APM
- **L2 Cache** : 256 KB (Celeron) ~ 512 KB (Pentium III)
- **DRAM Memory** : Onboard SODIMM socket up to 512MB of SDRAM
- **Enhanced IDE with UltraDMA** : supports 2 port and up to 4 ATAPI devices, Ultra DMA transfer 33 / 66 and 100 MB/sec.
- **Real-time Clock** : built-in chipset with lithium battery backup(built on carrier board). CMOS data backup of BIOS setup and BIOS default.

### High Speed Multi I/O

- **Chipset** : VIA VT82C686B
- **Serial Ports** : Two high speed RS-232C ports (COM1). One high speed RS-232C/422/485 port COM2 (jumper selectable). Both with 16C550 compatible UART and 16 byte FIFO.
- **USB** : 4 onboard USB ver 1.1 ports
- **SIR Interface** : onboard IrDA TX/RX port
- **Bi-directional Parallel Port** : SPP, EPP and ECP mode.
- **Keyboard and Mouse** : support one PS/2 Keyboard and one PS/2 Mouse
- **Audio Chipset**: VIA VT82C686B, AC97 2.0 compliant, Multistream Direct Sound and Direct Sound 3D acceleration.

---

## Network Interface Controller

- **Chipset** : Realtek 8139C, 10/100 Mbps

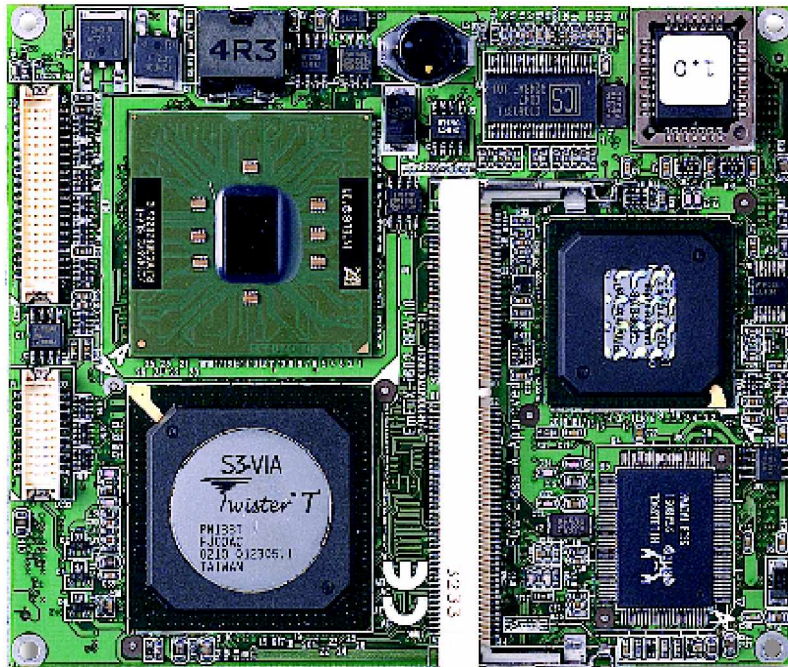
## Display Controller

- **Chipset** : 4x AGP S3 Savage4 3D and S3 Savage 2000 2D engines integrated in VT8606 supports up to 32MB of Shared Memory
- **Display Type** : Flat Panel and CRT displays up to 1280x1024 @ 32 bpp
  - Lcd interface : Flat Panel 36-bit TFT/DSTN interface
  - LVDS interface(PBE-1000) : Scalable Bandwidth is ranging from 25MHz~112MHz(VGA~SXGA) 18/36-bit one/two channel LVDS interface
  - TV-Out : Support NTSC,PAL NTSC-EIA(Japan) formats . Support 640x480 resolutions
- **Resolution**: Single Channel of LVDS / 36-bit of TTL and 12-bit of TMDS; all resolutions are supported up to 1280x1024.

## Environmental and Power

- **Power Requirements** : +5 V @ 2.18 A (typical);(Low Power Embedded Celeron 400MHz and 512MB SDRAM)
- **System Monitoring and Alarm** : CPU and System temperature, system voltage .
- **Board Dimensions** : 95mm x 114mm (3.7" x 4.5")
- **Board Weight** : 0.087kg
- **Operating Temperature** : 0 to 60°C (32 to 140°F)

Board Image



# Warning

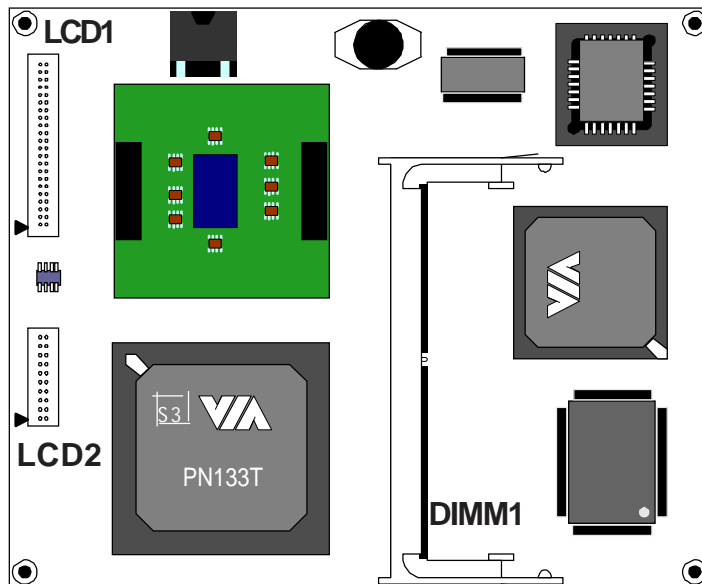
Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside
2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry
3. Use a grounded wrist strap when handling computer components.
4. Place components on a grounded antistatic pad or on the bag that came with the Single Board Computer, whenever components are separated from the system

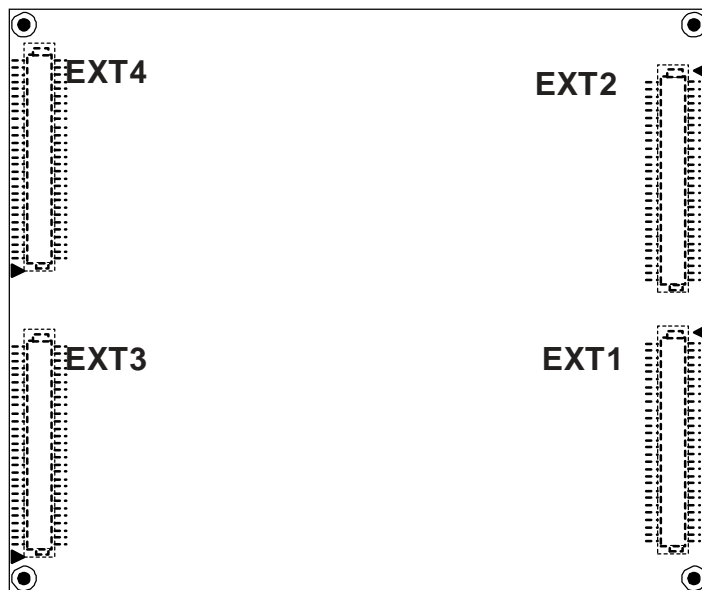
## Ordering Codes

<b>3312390</b>	ETX Embedded Intel Celeron ULV 400MHz Single Board Computer with one SODIMM socket up to 512 MB SDRAM, CRT SVGA, One Realtek 8139C Fast Ethernet, AC97 3D Audio.	
<b>3312390C</b>	ETX Embedded Intel PIII Tualatin Low Power 800MHz Single Board Computer with one SODIMM socket up to 512 MB SDRAM, CRT SVGA, One Realtek 8139C Fast Ethernet, AC97 3D Audio.	
<b>1001010</b>	The Evaluation Board for ETX serials development (ATX form factor)	
<b>Heat Sink</b>	2631040950001	
<b>SODIMM</b>	64MB	5150064001440
	128MB	5150128001440

## Board Layout Front



## Board Layout View (Back)



## Jumper/Connector Quick Reference

Connectors	
Lable	Function
LCD1	LCD TTL Connector 1
LCD2	LCD TTL Connector 2
ETX1	PCI Bus, USB, Audio
ETX2	ISA Bus
ETX3	VGA,LCD,Video,COM1,COM2,LPT,IrDA,M/K
ETX4	IDE1,IDE2,Ethernet,Miscellaneous

---

## Watchdog Timer

### Watchdog Output

The onboard watchdog timer can be disabled by jumper setting or enabled for either reboot by system RESET. The Jumper is on the carrier board.

Even if enabled by jumper setting upon boot the watchdog timer is always inactive. To initialize or refresh the watchdog timer writing of port 444H is sufficient. To disable the watchdog timer read port 44H.

Status	Action
Enable/refresh the Watchdog Timer	I/O Write 444H
Disable the Watchdog Timer.	I/O Read 044H

After the watchdog timer has been initialized by reading port 444H, it has to be strobed at preconfigured intervals to keep it from issuing a RESET or NMI.

The watchdog timer timeout intervals are set by software programming.

### Timeout Values

Timeout values are programmed. The watchdog timer supports 255 steps. Use the table on the next page to find the hexadecimal value that needs to be passed on to get the correct timer interval. Look subsequently at the program example how to pass the value to the watchdog timer.

### Timeout Table

Level	Value	Seconds	Level	Value	Seconds	Level	Value	Seconds
1	1	1	2	2	2	3	3	3
4	4	4	5	5	5	6	6	6
7	7	7	8	8	8	9	9	9
10	A	10	11	B	11	12	C	12
13	D	13	14	E	14	15	F	15
16	10	16	17	11	17	18	12	18
19	13	19	20	14	20	21	15	21

---

22	16	22	23	17	23	24	18	24
25	19	25	26	1A	26	27	1B	27
28	1C	28	29	1D	29	30	1E	30
31	1F	31	32	20	32	33	21	33
34	22	34	35	23	35	36	24	36
37	25	37	38	26	38	39	27	39
40	28	40	41	29	41	42	2A	42
43	2B	43	44	2C	44	45	2D	45
46	2E	46	47	2F	47	48	30	48
49	31	49	50	32	50	51	33	51
52	34	52	53	35	53	54	36	54
55	37	55	56	38	56	57	39	57
58	3A	58	59	3B	59	60	3C	60
61	3D	61	62	3E	62	63	3F	63
64	40	64	65	41	65	66	42	66
67	43	67	68	44	68	69	45	69
70	46	70	71	47	71	72	48	72
73	49	73	74	4A	74	75	4B	75
76	4C	76	77	4D	77	78	4E	78
79	4F	79	80	50	80	81	51	81
82	52	82	83	53	83	84	54	84
85	55	85	86	56	86	87	57	87
88	58	88	89	59	89	90	5A	90
91	5B	91	92	5C	92	93	5D	93
94	5E	94	95	5F	95	96	60	96
97	61	97	98	62	98	99	63	99
100	64	100	101	65	101	102	66	102
103	67	103	104	68	104	105	69	105
106	6A	106	107	6B	107	108	6C	108
109	6D	109	110	6E	110	111	6F	111
112	70	112	113	71	113	114	72	114
115	73	115	116	74	116	117	75	117
118	76	118	119	77	119	120	78	120
121	79	121	122	7A	122	123	7B	123
124	7C	124	125	7D	125	126	7E	126
127	7F	127						

---

## Programming Example

The following program is an examples of how to enable, disable and refresh the Watchdog timer:

```
WDT_EN_RF      equ      444H

WDT_DIS equ     044h

WT_Enable      push AX          ; Save AX,DX
                push DX
                mov DX,WDT_EN_RF ; Enable Timer
                mov AX,INTERVAL ; Set Timeout Value
                out DX,AX
                pop DX           ; Restore DX,AX
                pop AX
                ret

WT_Refresh     push AX          ; Save AX,DX
                push DX
                mov DX,WDT_EN_RF ; Refresh Timer
                mov AX,INTERVAL ; Set Timeout Value
                out DX,AX
                pop DX           ; Restore DX,AX
                pop AX
                ret

WT_Disable     push AX          ; Save AX,DX
                push DX
                mov DX,WDT_DIS   ; Disable Timer
                in AX,DX
                pop DX           ; Restore DX,AX
                pop AX
                ret

WT_Disable     push AX          ; save AX,DX
                push DX
                mov DX,WDT_DIS   ; Disable Timer
                in AX,DX
                pop DX           ; restore DX,AX
                pop AX
                ret
```

---

## Flat Panel VGA

### LCD1

Type : Onboard 40-pin Box Header (Hirose DF-40DS-1.25C)

Pin	Description	Pin	Description
1	VCC5V	2	VCC5V
3	GND	4	GND
5	VCC3V	6	VCC3V
7	NC	8	GND
9	FPD0	10	FPD1
11	FPD2	12	FPD3
13	FPD4	14	FPD5
15	FPD6	16	FPD7
17	FPD8	18	FPD9
19	FPD10	20	FPD11
21	FPD12	22	FPD13
23	FPD14	24	FPD15
25	FPD16	26	FPD17
27	FPD18	28	FPD19
29	FPD20	30	FPD21
31	FPD22	32	FPD23
33	GND	34	GND
35	SHFCLK	36	PANELHS
37	M(DE)	38	PANELVS
39	ENABLK	40	ENAVEE

### LCD2

Type : Onboard 20-pin Box Header (Hirose DF-20DS-1.25C)

Pin	Description	Pin	Description
1	GND	2	GND
3	FPD24	4	FPD25
5	FPD26	6	FPD27
7	FPD28	8	FPD29
9	FPD30	10	FPD31
11	FPD32	12	FPD33
13	FPD34	14	FPD35
15	GND	16	GND
17	NC	18	NC
19	NC	20	NC

---

## System Resources

### *Interrupt Assignment*

<b>IRQ Address</b>	<b>Description</b>
0	System Timer
1	Keyboard (KB output buffer full)
2	Programmable Interrupt Controller
3	Serial Port 2 (COM2)
4	Serial Port 1 (COM1)
5	AC'97 Audio for VIA Audio Controller
6	Reversed
7	Parallel Port 1
8	Real-Time Clock
9	VIA Tech 3038 PCI To USB Universal Host Controller
10	S3 Graphics Twister
11	Realtek RTL 8139(A/B/C/8130) PCI Fast Ethernet NIC
12	PS/2 Mouse
13	Numeric data processor
14	Primary IDE Controller
15	Secondary IDE Controller

### *I/O Address Space*

<b>Adress</b>	<b>Description</b>
0000 - 000F	DMA Controller
0010 - 001F	Motherboard Resources
0020 - 0021	PIC
0022 - 003F	Motherboard Resources
0040 - 0043	System Timer
0044 - 005F	Motherboard Resources
0060 - 0060	Keyboard
0061 - 0061	Systems Speaker
0062 - 0063	Motherboard Resources
0064 - 0064	Keyboard
0065 - 006F	Motherboard Resources
0070 - 0073	System CMOS / Real time clock
0074 - 007F	Motherboard Resources

---

0080 - 0090	DMA Controller
0091 - 0093	Motherboard Resources
0094 - 009F	DMA Controller
00A0 - 00A1	PIC
00A2 - 00BF	Motherboard Resources
00E0 - 00BF	Motherboard Resources
00C0 - 00DF	DMA Controller
00F0 - 00FF	Numeric Data Processor
0170 - 0177	VIA Bus Master PCI IDE Controller
01F0 - 01F7	VIA Bus Master PCI IDE Controller
02F8 - 02FF	Communications (COM2)
0376 - 0376	VIA Bus Master PCI IDE Controller
0378 - 037F	Printer Port (LPT1)
03B0 - 03BB	S3 Graphics Twister
03C0 - 03DF	S3 Graphics Twister
03F6 - 03F6	VIA Bus Master PCI IDE Controller
03F7 - 03F7	Floppy Disk Controller
03F8 - 03FF	Communications (COM1)
04D0 - 04D1	Motherboard Resources
0CF8 - 607F	PCI Bus
D000 - D00F	VIA Bus Master PCI IDE Controller
D400 - D41F	VIA Tech 3038 PCI to USB Universal Host Controller
D800 - D81F	VIA Tech 3038 PCI to USB Universal Host Controller
DC00 - DCFF	Avance AC'97 Audio for VIA (R) Audio Controller
E000 - E003	Avance AC'97 Audio for VIA (R) Audio Controller
E400 - E403	Avance AC'97 Audio for VIA (R) Audio Controller
E800 - E8FF	Realtek RTL8139(A/B/C/8130) PCI Fast Ethernet NIC

## ETX Connector

### ETX1

### ETX2

1	GND	GND	2	1	GND	GND	2
3	PCICLK3	PCICLK4	4	3	SD14	SD15	4
5	GND	GND	6	5	SD13	MASTER#	6
7	PCICLK1	PCICLK2	8	7	SD12	DREQ7	8
9	REQ#3	GNT#3	10	9	SD11	DACK#7	10
11	GNT#2	VCC3	12	11	SD10	DREQ6	12
13	REQ#2	GNT#1	14	13	SD9	DACK#6	14
15	REQ#1	VCC3	16	15	SD8	DREQ5	16
17	GNT#0	N.C	18	17	MEMW#	DACK#5	18
19	VCC	VCC	20	19	MEMR#	DREQ0	20
21	SERIRQ	REQ#0	22	21	LA17	DACK#0	22
23	AD0	VCC3	24	23	LA18	IRQ14	24
25	AD1	AD2	26	25	LA19	IRQ15	26
27	AD4	AD3	28	27	LA20	IRQ12	28
29	AD6	AD5	30	29	LA21	IRQ11	30
31	CBE#0	AD7	32	31	LA22	IRQ10	32
33	AD8	AD9	34	33	LA23	IO16#	34
35	GND	GND	36	35	GND	GND	36
37	AD10	AUXAL	38	37	SBHE#	M16#	38
39	AD11	MIC	40	39	SA0	OSC	40
41	AD12	AUXAR	42	41	SA1	BALE	42
43	AD13	ASVCC	44	43	SA2	TC	44
45	AD14	SNDL	46	45	SA3	DACK#2	46
47	AD15	ASGND	48	47	SA4	IRQ3	48
49	CBE#1	SNDR	50	49	SA5	IRQ4	50
51	VCC	VCC	52	51	VCC	VCC	52
53	PAR	SERR#	54	53	SA6	IRQ5	54
55	PERR#	N.C	56	55	SA7	IRQ6	56
57	PME#	USB2-	58	57	SA8	IRQ7	58
59	LOCK#	DEVSEL#	60	59	SA9	SYSCLK	60
61	TRDY#	USB3-	62	61	SA10	REFCH#	62
63	IRDY#	STOP#	64	63	SA11	DREQ1	64
65	FRAME#	USB2+	66	65	SA12	DACK#1	66
67	GND	GND	68	67	GND	GND	68
69	AD16	CBE#2	70	69	SA13	DREQ3	70
71	AD17	USB3+	72	71	SA14	DACK#3	72
73	AD19	AD18	74	73	SA15	IOR#	74
75	AD20	USB0-	76	75	SA16	IOW#	76
77	AD22	AD21	78	77	SA18	SA17	78
79	AD23	USB1-	80	79	SA19	SMEMR#	80
81	AD24	CBE#3	82	81	IOCHRDY	AEN	82
83	VCC	VCC	84	83	VCC	VCC	84
85	AD25	AD26	86	85	SD0	SMEMW#	86
87	AD28	USB0+	88	87	SD2	SD1	88
89	AD27	AD29	90	89	SD3	NOWS#	90
91	AD30	USB1+	92	91	DREQ2	SD4	92
93	PCIRST#	AD31	94	93	SD5	IRQ9	94
95	INTR#C	INTR#D	96	95	SD6	SD7	96
97	INTR#A	INTR#B	98	97	IOCHK#	RSTDRV	98
99	GND	GND	100	99	GND	GND	100

## ETX Connector

### ETX3

### ETX4

1	GND	GND	2	1	GND	GND	2
3	R	B	4	3	SV_SB	PWGIN	4
5	HSY	G	6	5	PS_ON	SPEAKER	6
7	VSY	DDCK	8	7	PWRBTN#	BATT	8
9	N.C/DE	DDDA	10	9	KBINH	LILED	10
11	LCD16/B4	LCD18/B2	12	11	WDTRIG	ACTLED	12
13	LCD17/B5	LCD19/B3	14	13	ROMKBCS#	SPEEDLED	14
15	GND	GND	16	15	EXT_PRG	12CLK	16
17	LCD13/B1	LCD15/B3	18	17	VCC	VCC	18
19	LCD12/B0	LCD14/B2	20	19	OVCR#	GPCS#	20
21	GND	GND	22	21	EXTSMI#	12DAT	22
23	LCD8/G2	LCD11/G5	24	23	SMBCLK	SMBDAT	24
25	LCD9/G3	LCD10/G0	26	25	SIDE_CS3#	CPU_FAN	26
27	GND	GND	28	27	SIDE_CS1#	DASP_S	28
29	LCD4/R4	LCD7/G1	30	29	SIDE_A2	PIDE_CS3#	30
31	LCD5/R5	LCD6/G0	32	31	SIDE_A0	PIDE_CS1#	32
33	GND	GND	34	33	GND	GND	34
35	LCD1/R1	LCD3/R3	36	35	PDIAG_S	PIDE_A2	36
37	LCD0/R0	LCD2/R2	38	37	SIDE_A1	PIDE_A0	38
39	VCC	VCC	40	39	SIDE_INTRQ	PIDE_A1	40
41	JILI_DAT	LTGIO0	42	41	N.C	N.C	42
43	JILI_CLK	BLON#	44	43	SIDE_ACK#	PIDE_INTRQ	44
45	BIASON	DIGON	46	45	SIDE_RDY	PIDE_ACK#	46
47	COMP	Y	48	47	SIDE_IOR#	PIDE_RDY	48
49	SYNC	C	50	49	VCC	VCC	50
51	LPT/FLPY#	N.C/SHFCLK	52	51	SIDE_IOW#	PIDE_IOR#	52
53	VCC	GND	54	53	SIDE_DRQ	PIDE_IOW#	54
55	STB#/I.C	AFD#/DENSEL	56	55	SIDE_D15	PIDE_DRQ	56
57	I.C	PD7/N_C	58	57	SIDE_D0	PIDE_D15	58
59	IRRX	ERR#/HDSSEL#	60	59	SIDE_D14	PIDE_D0	60
61	IRTX	PD6/MOT0	62	61	SIDE_D1	PIDE_D14	62
63	RXD2	INIT#/DIR#	64	63	SIDE_D13	PIDE_D1	64
65	GND	GND	66	65	GND	GND	66
67	RTS#2	PD5/N.C	68	67	SIDE_D2	PIDE_D13	68
69	DTR#2	SLIN#/STEP#	70	69	SIDE_12	PIDE_D2	70
71	DCD#2	PD4/DSKCHG#	72	71	SIDE_D3	PIDE_D12	72
73	DSR#2	PD3/RDATA#	74	73	SIDE_D11	PIDE_D3	74
75	CTS#2	PD2/WP#	76	75	SIDE_D4	PIDE_D11	76
77	TXD#2	PD1/TRK0#	78	77	SIDE_D10	PIDE_D4	78
79	RI#2	PD0/INDEX#	80	79	SIDE_D5	PIDE_D10	80
81	VCC	VCC	82	81	VCC	VCC	82
83	RXD1	ACK#/I.C	84	83	SIDE_D9	PIDE_D5	84
85	RTS#1	BUSY#/I.C	86	85	SIDE_D6	PIDE_D9	86
87	DTR#1	PE/WDATA#	88	87	SIDE_D8	PIDE_D6	88
89	DCD#1	SLCT#/WGATE#	90	89	-RI	LAN_WAKE	90
91	DSR#1	MSCLK	92	91	RXD-	PIDE_D8	92
93	CTS#1	MSDAT	94	93	RXD+	SIDE_D7	94
95	TXD#1	KBCLK	96	95	TXD-	PIDE_D7	96
97	RI#1	KBDAT	98	97	TXD+	HDRST#	98
99	GND	GND	100	99	GND	GND	100

---

## AWARD BIOS Setup

The SBC uses the Award PCI/ISA BIOS ver 6.0 for the system configuration. The Award BIOS setup program is designed to provide the maximum flexibility in configuring the system by offering various options which could be selected for end-user requirements. This chapter is written to assist you in the proper usage of these features.

To access AWARD PCI/ISA BIOS Setup program, press <Del> key. The Main Menu will be displayed at this time.



Once you enter the AwardBIOS™ CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to accept and enter the sub-menu.

---

## Setup Items

The main menu includes the following main setup categories. Recall that some systems may not include all entries.

### **Standard CMOS Features**

Use this menu for basic system configuration.

### **Advanced BIOS Features**

Use this menu to set the Advanced Features available on your system.

### **Advanced Chipset Features**

Use this menu to change the values in the chipset registers and optimize your system's performance.

### **Integrated Peripherals**

Use this menu to specify your settings for integrated peripherals.

### **Power Management Setup**

Use this menu to specify your settings for power management.

### **PnP / PCI Configuration**

This entry appears if your system supports PnP / PCI.

### **PC Health Status**

This entry appears CPU temperature for the system.

### **Frequency/Voltage Control**

Use this menu to specify your settings for frequency/voltage control.

### **Load Optimized Defaults**

Use this menu to load the BIOS default values that are factory settings for optimal performance system operations. While Award has designed the custom BIOS to maximize performance, the factory has the right to change these defaults to meet their needs.

### **Set Password**

Use this menu to set User and Supervisor Passwords.

### **Save & Exit Setup**

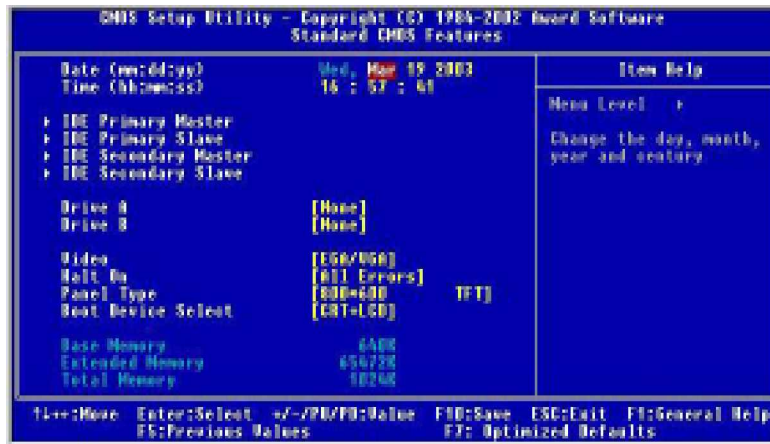
Save CMOS value changes to CMOS and exit setup.

### **Exit Without Save**

Abandon all CMOS value changes and exit setup.

---

## Standard CMOS Setup



↑↓ → ←: Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: General Help  
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

### Date

The BIOS determines the day of the week from the other date information; this field is for information only.

### Time

The time format is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Press the « or ( key to move to the desired field. Press the PgUp or PgDn key to increment the setting, or type the desired value into the field.

### IDE Primary Master/Slave

### IDE Secondary Master/Slave

Options are in sub menu (see page 30)

### Drive A, B

Select the correct specifications for the diskette drive(s) installed in the computer.

<b>None</b> ;	No diskette drive installed
<b>360K</b> ;	5.25 in 5-1/4 inch PC-type standard drive
<b>1.2M</b> ;	5.25 in 5-1/4 inch AT-type high-density drive
<b>720K</b> ;	3.5 in 3-1/2 inch double-sided drive
<b>1.44M</b> ;	3.5 in 3-1/2 inch double-sided drive
<b>2.88M</b> ;	3.5 in 3-1/2 inch double-sided drive

---

**Video** Select the type of primary video subsystem in your computer. The BIOS usually detects the correct video type automatically. The BIOS supports a secondary video subsystem, but you do not select it in Setup.

**Halt On** During the power-on self-test (POST), the computer stops if the BIOS detects a hardware error. You can tell the BIOS to ignore certain errors during POST and continue the boot-up process. These are the selections:

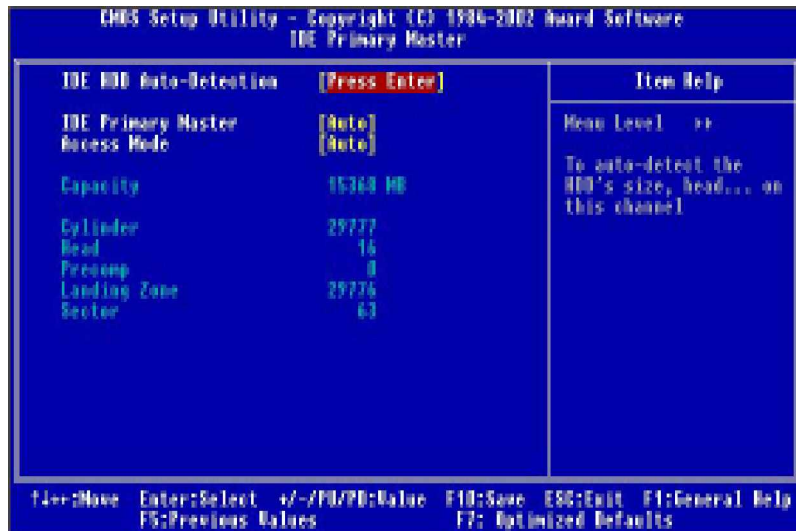
No errors	POST does not stop for any errors.
All errors	If the BIOS detects any non-fatal error, POST stops and prompts you to take corrective action.
All, But Keyboard	POST does not stop for a keyboard error, but stops for all other errors.
All, But Diskette	POST does not stop for diskette drive errors, but stops for all other errors.
All, But Disk/Key	POST does not stop for a keyboard or disk error, but stops for all other errors.

**Panel Type** Select the different panel type to run the system. Four various resolutions for TFT type and two for DSTN.

**Boot Device** This item allows you to select the different devices for boot up function

---

## IDE Harddisk Setup (submenu)



↑↓←→:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help  
F5:Previous Values F6:Fail-Safe Defaults F7:Optimized Defaults

### IDE HDD Auto-detection

Press Enter to auto-detect the HDD on this channel. If detection is successful, it fills the remaining fields on this menu.

### IDE Primary Master

Selecting 'manual' lets you set the remaining fields on this screen. Selects the type of fixed disk. "User Type" will let you select the number of cylinders, heads, etc. Note: PRECOMP=65535 means NONE !

### Capacity

Disk drive capacity (Approximated). Note that this size is usually slightly greater than the size of a formatted disk given by a disk checking program.

### Access Mode

Normal, LBA, Large or Auto Choose the access mode for this hard disk

---

The following options are selectable only if the 'IDE Primary Master' item is set to 'Manual'

**Cylinder**           Min = 0   Max = 65535  
Set the number of cylinders for this hard disk.

**Head**                Min = 0   Max = 255  
Set the number of read/write heads

**Precomp**            Min = 0   Max = 65535  
\*\*\*\* Warning: Setting a value of 65535 means no hard disk

**Landing zone**      Min = 0   Max = 65535  
\*\*\*\* Warning: Setting a value of 65535 means no hard disk

**Sector**             Min = 0   Max = 255  
Number of sectors per track

We recommend that you select Type "AUTO" for all drives. The BIOS will auto-detect the hard disk drive and CD-ROM drive at the POST stage.

If your hard disk drive is a SCSI device, please select "None" for your hard drive setting.

## BIOS Features Setup



↑↓ → ←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help  
F5:Previous Values F6:Fail-Safe Defaults F7:Optimized Defaults

### Virus Warning

Allows you to choose the VIRUS Warning feature for IDE Hard Disk boot sector protection. If this function is enabled and someone attempt to write data into this area, BIOS will show a warning message on screen and beep.

Enabled Activates automatically when the system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table.

Disabled No warning message will appear when anything attempts to access the boot sector or hard disk partition table.

---

**CPU Internal Cache/External Cache**

These two categories speed up memory access. However, it depends on CPU/chipset design. Enabled : Enable cache, Disabled : Disable cache

**CPU L2 Cache ECC Checking**

This item allows you to enable/disable CPU L2 Cache ECC checking.  
The choice: Enabled, Disabled.

**Processor Number Feature**

This feature appears when a Pentium III processor is installed. It enables you to control whether the Pentium III's serial number can be read by external programs. The choice : Enabled. Disabled

**Quick Power On Self Test**

This category speeds up Power On Self Test (POST) after you power up the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST. Enabled : Enable quick POST. Disabled : Normal POST

**First/Second/Third/Other Boot Device**

The BIOS attempts to load the operating system from the devices in the sequence selected in these items. The choices are : Floppy, LS/ZIP, HDD, SCSI, CDROM, Disabled.

**Swap Floppy Drive**

If the system has two floppy drives, you can swap the logical drive name assignments. The choice: Enabled/Disabled.

**Boot Up Floppy Seek**

Seeks disk drives during boot up. Disabling speeds boot up.  
The choice: Enabled/Disabled.

**Boot Up NumLock Status**

Select power on state for NumLock. The choice: Enabled/Disabled.

**Gate A20 Option**

Select if chipset or keyboard controller should control GateA20.  
Normal A pin in the keyboard controller controls GateA20  
Fast Lets chipset control GateA20

**Typematic Rate Setting**

Key strokes repeat at a rate determined by the keyboard controller. When enabled, the typematic rate and typematic delay can be selected.  
The choice: Enabled/Disabled.

**Typematic Rate (Chars/Sec)**

Sets the number of times a second to repeat a key stroke when you hold the key down. The choice: 6, 8, 10, 12, 15, 20, 24, 30.

**Typematic Delay (Msec)**

Sets the delay time after the key is held down before it begins to repeat the keystroke. The choice: 250, 500, 750, 1000.

---

**Security Option**

Select whether the password is required every time the system boots or only when you enter setup.

**System** The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.

**Setup** The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

**Note** To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and just press <Enter>, it will disable security. Once the security is disabled, the system will boot and you can enter Setup freely.

**OS Select For DRAM > 64MB**

Select the operating system that is running with greater than 64MB of RAM on the system. The choice: Non-OS2, OS2.

**Video BIOS Shadow**

Enabled this copies the video BIOS from ROM to RAM. effectively enhancing performance, and reducing the amount of upper memory available by 32KB (the C0000-C7FFF area of memory between 640 KB and 1 MB is used).

**C8000-CBFFF Shadow**

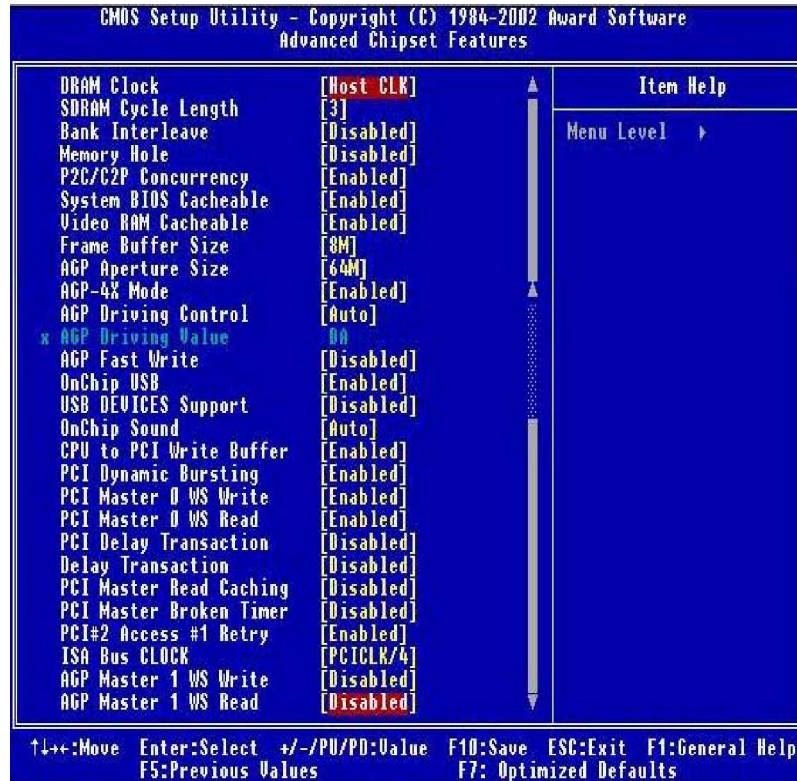
Enabling any of the C8000-CBFFF segments allows components to move their firmware into these upper memory segments. However your computer can lock-up doing so, because some devices don't like being shadowed at those particular 16 KB segments of upper memory.

**Note** - In Windows 95, double click 'Computer' within Device Manager and select 'Memory'. This will tell you what segments (if any) are being shadowed. For DOS you can use MSD.EXE to see what segments are claimed.

CC000-CFFFF - D0000-D3FFF - D4000-D7FFF - D8000-DBFFF and  
DC000-DFFFF - Same as above.

---

## Chipset Features Setup



↑↓←→:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help  
F5:Previous Values F6:Fail-SAFE Defaults F7:Optimized Defaults

### DRAM Clock

This item allows you to set the DRAM Clock. Options are Host CLK, HCLK+33M or HCLK-33M. Please set the item according to the Host (CPU) Clock and DRAM Clock.

### SDRAM Cycle Length

This feature is similar to SDRAM CAS Latency Time. It controls the time delay (in clock cycles - CLKs) that passes before the SDRAM starts to carry out a read command after receiving it. This also determines the number of CLKs for the completion of the first part of a burst transfer. Thus, the lower the cycle length, the faster the transaction. However, some SDRAM cannot handle the lower cycle length and may become unstable. So, set the SDRAM Cycle Length to 2 for optimal performance if possible but increase it to 3 if your system becomes unstable.

---

**Bank Interleave**

This feature enables you to set the interleave mode of the SDRAM interface. Interleaving allows banks of SDRAM to alternate their refresh and access cycles. One bank will undergo its refresh cycle while another is being accessed. This improves performance of the SDRAM by masking the refresh time of each bank. A closer examination of interleaving will reveal that since the refresh cycles of all the SDRAM banks are staggered, this produces a kind of pipelining effect. If there are 4 banks in the system, the CPU can ideally send one data request to each of the SDRAM banks in consecutive clock cycles. This means in the first clock cycle, the CPU will send an address to Bank 0 and then send the next address to Bank 1 in the second clock cycle before sending the third and fourth addresses to Banks 2 and 3 in the third and fourth clock cycles respectively. Each SDRAM DIMM consists of either 2 banks or 4 banks. 2-bank SDRAM DIMMs use 16Mbit SDRAM chips and are usually 32MB or less in size. 4-bank SDRAM DIMMs, on the other hand, usually use 64Mbit SDRAM chips though the SDRAM density may be up to 256Mbit per chip. All SDRAM DIMMs of at least 64MB in size or greater are 4-banked in nature.

If you are using a single 2-bank SDRAM DIMM, set this feature to 2-Bank. But if you are using two 2-bank SDRAM DIMMs, you can use the 4-Bank option as well. With 4-bank SDRAM DIMMs, you can use either interleave options. Naturally, 4-bank interleave is better than 2-bank interleave so if possible, set it to 4-Bank. Use 2-Bank only if you are using a single 2-bank SDRAM DIMM. Notethat it is recommends that SDRAM bank interleaving be disabled if 16Mbit SDRAM DIMMs are used.

**Memory Hole**

Enabling this feature reserves 15MB to 16MB memory address space to ISA expansion cards that specifically require this setting. This makes the memory from 15MB and up unavailable to the system. Expansion cards can only access memory up to 16MB.

**P2C/C2P Concurrency**

When Disabled, CPU bus will be occupied during the entire PCI operation period.

**System BIOS Cacheable**

Allows the system BIOS to be cached for faster system performance.

**Video RAM Cacheable**

This item allows you to "Enabled" or "Disabled" on Video RAM Cacheable.

**Frame Buffer Size**

This item defines the amount of system memory that will be shared and uses as video memory.

---

**AGP Aperture Size**

Options : 4, 8, 16, 32, 64, 128, 256

This option selects the size of the AGP aperture. The aperture is a portion of the PCI memory address range dedicated as graphics memory address space. Host cycles that hit the aperture range are forwarded to the AGP without need for translation. This size also determines the maximum amount of system RAM that can be allocated to the graphics card for texture storage.

AGP Aperture size is set by the formula : maximum usable AGP memory size x 2 plus 12MB. That means that usable AGP memory size is less than half of the AGP aperture size. That's because the system needs AGP memory (uncached) plus an equal amount of write combined memory area and an additional 12MB for virtual addressing. This is address space, not physical memory used. The physical memory is allocated and released as needed only when Direct3D makes a "create non-local surface" call.

**AGP-4X Mode**

Set to Enabled if your AGP card supports the 4X mode, which transfers video data at 1066MB/s.

**AGP Driving Control**

This item is use for control AGP drive strength.

Auto: Setup AGP drive strength by default setting.

Manual: Setup AGP drive strength by manual setting.

**AGP Driving Value**

Key in a HEX number to control AGP output buffer drive strength.

Min = 00, Max = FF.

**AGP Fast Write**

To enable this function can increase VGA performance on graphic designed..

**OnChip USB**

If your system contains a Universal Serial Bus controller and you have a USB peripheral, select Enabled. The next option will become available.

**USB Legacy Support**

Enable this item to support USB devices booting.

**OnChip Sound**

This menu can access the sound controller automaticlly

---

#### **CPU to PCI Write Buffer**

This controls the CPU write buffer to the PCI bus. If this buffer is disabled, the CPU writes directly to the PCI bus. Although this may seem like the faster and thus, the better method, this isn't true. Because the CPU bus is faster than the PCI bus, any CPU writes to the PCI bus has to wait until the PCI bus is ready to receive data. This prevents the CPU from doing anything else until it has completed sending the data to the PCI bus. Enabling the buffer enables the CPU to immediately write up to 4 words of data to the buffer so that it can continue on another task without waiting for those 4 words of data to reach the PCI bus. The data in the write buffer will be written to the PCI bus when the next PCI bus read cycle starts. The difference here is that it does so without stalling the CPU for the entire CPU to PCI transaction. Therefore, it's recommended that you enable the CPU to PCI write buffer.

#### **PCI Dynamic Bursting**

When enabled, data transfer on the PCI bus, where possible, make use of the high-performance PCI burst protocol, in which greater amounts of data are transferred at a single command.

#### **PCI Master 0 WS Write**

This function determines whether there's a delay before any writes to the PCI bus. If this is enabled, then writes to the PCI bus are executed immediately (with zero wait states), as soon as the PCI bus is ready to receive data. But if it is disabled, then every write transaction to the PCI bus is delayed by one wait state. Normally, it's recommended that you enable this for faster PCI performance. However, disabling it may be useful when overclocking the PCI bus results in instability. The delay will generally improve the overclockability of the PCI bus.

#### **PCI Master 0 WS Read**

This function determines whether there's a delay before any reads to the PCI bus. If this is enabled, then reads to the PCI bus are executed immediately (with zero wait states), as soon as the PCI bus is ready to receive data. But if it is disabled, then every read transaction to the PCI bus is delayed by one wait state. Normally, it's recommended that you enable this for faster PCI performance. However, disabling it may be useful when overclocking the PCI bus results in instability. The delay will generally improve the overclockability of the PCI bus.

#### **PCI Delay Transaction**

The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI specification version 2.1.

#### **Delay Transaction**

The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI specification version 2.1.

---

**PCI Master Read Caching**

To enable this function, the CPU L2 cache will be used to cache PCI master reads. This boosts the performance of PCI master. It's recommend to disable this feature

**PCI Master Broken Timer**

To enable this feature allows for slower PCI bus mastering expansion cards.

**PCI # 2 Access # 1 Retry**

This BIOS feature is linked to the CPU to PCI Write Buffer. Normally, the CPU to PCI Write Buffer is enabled. All writes to the PCI bus are, as such, immediately written into the buffer, instead of the PCI bus. This frees up the CPU from waiting till the PCI bus is free. The data are then written to the PCI bus when the next PCI bus cycle starts.

There's a possibility that the buffer write to the PCI bus may fail. When that happens, this BIOS option determines if the buffer write should be reattempted or sent back for arbitration. If this BIOS option is enabled, then the buffer will attempt to write to the PCI bus until successful. If disabled, the buffer will flush its contents and register the transaction as failed. The CPU will have to write again to the write buffer. It is recommended that you enable this feature unless you have many slow PCI devices in your system. In that case, disabling this feature will prevent the generation of too many retries which may severely tax the PCI bus.

**ISA Bus Clock**

Allows you to set the speed of the ISA bus in fractions fo the PCI bus speed, so if the PCI bus is operating at its theroretical maximum, 33Mhz, PCICLK/3 would yield an ISA speed of 11Mhz. The choices: 7.159Mhz, PCICLK/4 and PCICLK/3.

**AGP Master 1 WS Write**

By default, the AGP busmastering device waits for at least 2 wait states or AGP clock cycles before it starts a write transaction. This BIOS option allows you to reduce the delay to only 1 wait state or clock cycle. For better AGP write performance, enable this option but disable it if you experience weird graphical anomalies like wireframe effects and pixel artifacts after enabling this option.

**AGP Master 1 WS Read**

By default, the AGP busmastering device waits for at least 2 wait states or AGP clock cycles before it starts a read transaction. This BIOS option allows you to reduce the delay to only 1 wait state or clock cycle. For better AGP read performance, enable this option but disable it if you experience weird graphical anomalies like wireframe effects and pixel artifacts after enabling this option.

---

## Integrated Peripherals



↑↓ → ←: Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: General Help  
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

### OnChip IDE Channel 0/1

Select "Enabled" to activate each on-board IDE channel separately, Select "Disabled", if you install an add-on IDE Control card

### IDE Prefetch Mode

Enable prefetching for IDE drive interfaces that support its faster drive accesses. If you are getting disk drive errors, change the setting to omit the drive interface where the errors occur. Depending on the configuration of your IDE subsystem, this field may not appear, and it does appear when the Internal PCI/IDE filed, above, is Disabled.

---

**Primary & Secondary Master/Slave PIO**

These four PIO fields let you set a PIO mode (0-4) for each of four IDE devices. When under "Auto" mode, the system automatically set the best mode for each device

**Primary & Secondary Master/Slave UDMA**

When set to "Auto" mode, the system will detect if the hard drive supports Ultra DMA mode.

**Init Display First**

Select "AGP" or "PCI Slot" for system to detect first when boot-up.

**IDE HDD Block Mode**

This feature enhances disk performance by allowing multi-sector data transfers and eliminates the interrupt handling time for each sector.

**Onboard LAN Boot ROM**

This feature allows you to run LAN Boot function. Select "Disabled" not to access this function

**Onboard LAN**

Select "Enabled" if your system contains a LAN port.

**EEPROM PROTECTION**

Select "Disabled" to read and write the onboard EEPROM (128Bytes) ,and "Enabled" is read only.

**Onboard Serial Port 1 & 2**

Select an address and corresponding interrupt for the first/second serial port. The default value for the first serial port is "3F8/IRQ4" and the second serial port is "2F8/IRQ3".

**UART 2 Mode**

This item allows you to select UART mode. The choices: IrDA, ASKIR, Normal.

**RxD, TxD Active**

This item allows you to determine the active of RxD, TxD. The choices: "Hi,Hi", "Lo,Lo", "Lo,Hi", "Hi,Lo".

**Onboard Parallel Port**

Select address and interrupt for the Parallel port.

**Onboard Parallel Mode**

Select an operating mode for the parallel port. Mode options are Normal, EPP, ECP, ECP/EPP.

**ECP Mode Use DMA**

Select a DMA channel if parallel Mode is set as ECP, ECP/EPP.

**Parallel Port EPP Type**

Select a EPP Type if parallel Port is set as EPP, ECP/EPP.

---

**Secondary I/O Controller**

Configuration options: Enabled and Disabled. When Enabled, will enable the secondary I/O controller(on carrier board) ,including FDC controller , COM3 and COM4. The default setting is "Disabled".

**FDC Controller**

Configuration options: Enabled and Disabled.Enable the Floppy Disk Controller. The default setting is "Enabled".

**Onboard Serial Port 3**

Configuration options: 2E8, 2F8, 3E8, 3F8 and Disabled.The default setting is "Disabled".

**Serial Port 3 Use IRQ**

Configuration options: IRQ3, IRQ4, IRQ10 and IRQ11. The default setting is "IRQ11".

**Onboard Serial Port 4**

Configuration options: 2E8, 2F8, 3E8, 3F8 and Disabled.The default setting is "Disabled".

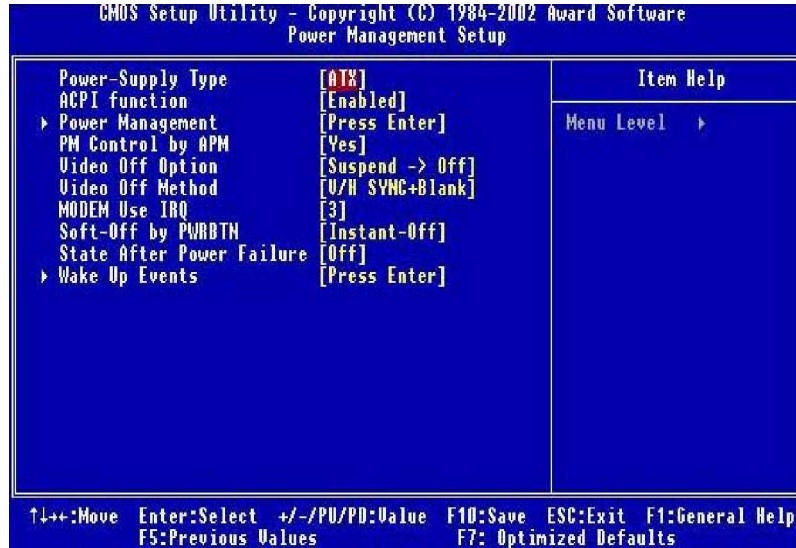
**Serial Port 4 Use IRQ**

Configuration options: IRQ3, IRQ4, IRQ10 and IRQ11. The default setting is "IRQ10".

**Onboard Legacy Audio**

Configuration options: Enabled and Disabled. When Enabled, select additional settings for SoundBlaster Compatibility and MPU-401 functionality

## Power Management Setup



### Power-Supply Type

Configuration options: ATX and AT . The item of "AT" is selected and the all of ACPI function will be hidden. The default setting is "ATX".

### ACPI Function

Select Enabled only if your computer's operating system supports ACPI (the Advanced Configuration and Power Interface) specification. Currently, Windows 98 and Windows2000 support ACPI.

### Power Management

There are 4 selections for Power Management, 3 of which have fixed mode :

- |                    |  |
|--------------------|--|
| Disabled (default) | No power management. Disables all four modes.  |
| Min. Power Saving  | Minimum power management. Doze Mode = 1 hr., Standby Mode = 1 hr., Suspend Mode = 1 hr.,                                   |
| Max. Power Saving  | Maximum power management -- ONLY AVAILABLE FOR SL CPU's.. Doze Mode = 1 min., Standby Mode = 1 min., Suspend Mode = 1 min. |
| User Defined       | Allows you to set each mode individually. When not disabled, each of the ranges are from 1 min. to 1 hr.                   |

HDD Power Down is always set independently

---

### **PM Control By APM**

When enabled, an Advanced power Management device will be activated to enhance the Max. Power Saving mode and stop the CPU internal clock. If the Max. Power Saving is not enabled, this will be preset to No.

### **Video Off Option**

Controls what causes the display to be switched off

Suspend -> Off                      Always On                      All Mode -> Off

### **Video Off Method**

This determines the manner in which the monitor is blanked.

V/H SYNC+Blank                      cause the system to turn off the vertical and horizontal synchronization signals and writes blanks to the screen.

Blank Screen                      This option only writes blanks to the screen.

DPMS                      Initial display power management signaling.

### **Modem Use IRQ**

Name the interrupt request (IRQ) assigned to the modem (if any) on your system. Activity of the selected IRQ always awakens the system.

### **Soft-Off By PWRBTN**

The field defines the power-off mode when using an ATX power supply. The Instant-Off mode means powering off immediately when pressing the power button. In the Delay 4 Sec mode, the system powers off when the power button is pressed for more than four seconds or places the system in a very low-power-usage state, with only enough circuitry receiving power to detect power button activity or resume by ring activity when press for less than four seconds. The default is 'Instant-Off'.

### **State After Power Failure**

This item allows you to select three status after the power failure. The choices are ON, OFF and Auto.

### **Wake Up Events**

Setting an event on each device listed to awaken the system from a soft off state.

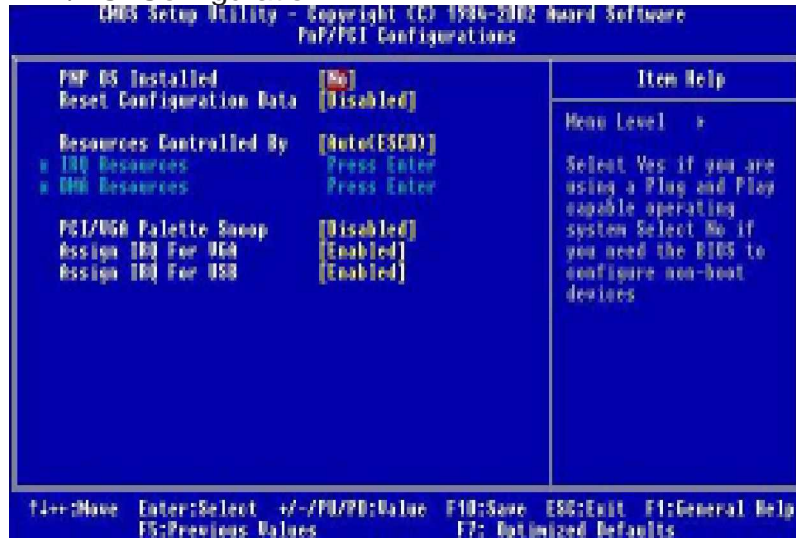
Power Button

Wake Up on LAN

Wake Up on Modem

RTC Alarm Resume

## PnP/PCI Configuration



↑↓ → ←: Move Enter: Select +/-/PU/PD: Value F10: Save ESC: Exit F1: General Help  
F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

This section describes configuring the PCI bus system. PCI, or Personal Computer Interconnect, is a system which allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own special components.

### PnP OS Installed

Select Yes if the system operating environment is Plug-and-Play aware (e.g., Windows 95).

### Reset Configuration Data

Normally, you leave this field Disabled. Select Enabled to reset ESCD (Extended System Configuration Data) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.

### Resource Controlled By

The Award Plug and Play BIOS can automatically configure all the boot and Plug-and-Play compatible devices. If you select Auto, all the interrupt request (IRQ) and DMA assignment fields disappear, as the BIOS automatically assigns them.

---

### **IRQ Resources**

When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt :

Legacy ISA     Devices compliant with the original PC/AT bus specification, requiring a specific interrupt (such as IRQ4 for serial port 1).

PCI/ISA PnP     Device compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

### **DMA Resources**

When resources are controlled manually, assign each system DMA channel as one of the following types, depending on the type of device using the DMA :

Legacy ISA     Devices compliant with the original PC/AT bus specification, requiring a specific DMA channel.

PCI/ISA PnP     Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

### **PCI/VGA Palette Snoop**

Normally this option is always Disabled! Nonstandard VGA display adapters such as overlay cards or MPEG video cards may not show colors properly. Setting Enabled should correct this problem. If this field set Enabled, any I/O access on the ISA bus to the VGA card's palette registers will be reflected on the PCI bus. This will allow overlay cards to adapt to the changing palette colors.

### **Assign IRQ For VGA**

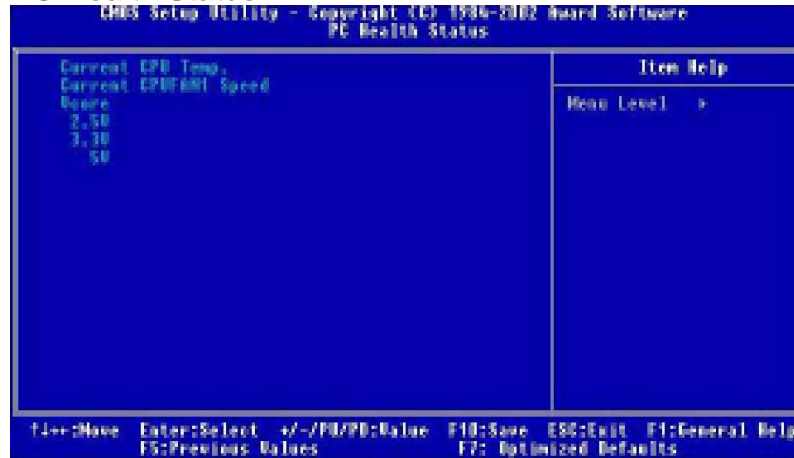
Many high-end graphics accelerator cards now require an IRQ to function properly. Disabling this feature with such cards will cause improper operation and/or poor performance. Thus, it's best to make sure you enable this feature if you are having problems with your graphics accelerator card. However, some low-end cards don't need an IRQ to run normally. Check your graphics card's documentation (manual). If it states that the card does not require an IRQ, then you can disable this feature to release an IRQ for other uses. When in doubt, it's best to leave it enabled unless you really need the IRQ.

### **Assign IRQ For USB**

Windows 95 will automatically give an IRQ to the USB port even if there is no USB peripheral connected. Disabling this will free the IRQ.

---

## PC Health Status



↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help  
F5:Previous Values F6:Fail-Safe Defaults F7:Optimized Defaults

This section describes CPU temperature for the system.

### **Current CPU Temp.**

Show you the current CPU temperature

### **Current CPUFAN Speed**

Show you the current CPUFAN operating speed

### **Vcore**

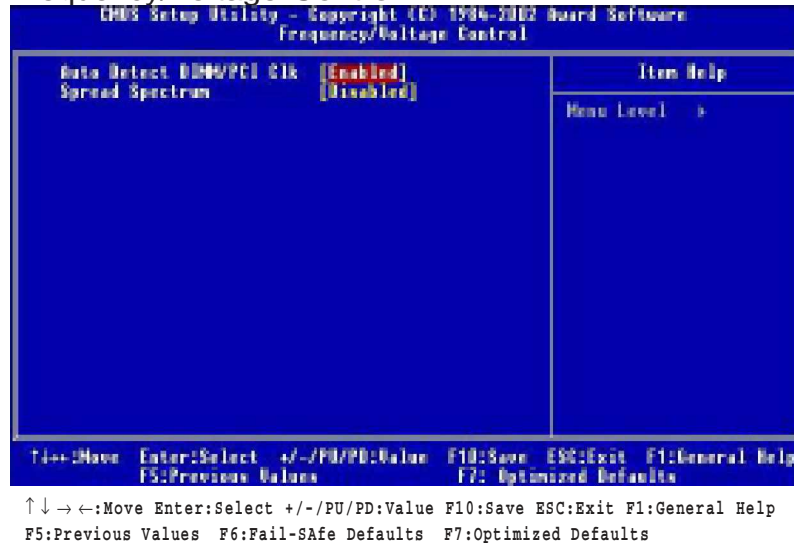
Show you one type of CPU voltage

### **+2.5, +3.3V, +5V**

Show you the different voltage can be used for the system

---

## Frequency/Voltage Control



This section describes Frequency and Voltage control for the system.

### Auto Detect DIMM/PCI CLK

When enabled, this item will auto detect if the DIMM and PCI socket have devices and will send clock signal to DIMM and PCI devices. When disabled, it will send the clock signal to all DIMM and PCI socket.

### Spread Spectrum

This item allows you to enable/disable the spread spectrum modulate.

---

## POST Codes

The following codes are not displayed on the screen. They can only be viewed on the LED display of a so called POST card. The codes are listed in the same order as the according functions are executed at PC startup. If you have access to a POST Card reader, you can watch the system perform each test by the value that's displayed. If the system hangs (if there's a problem) the last value displayed will give you a good idea where and what went wrong, or what's bad on the system board.

<b>CODE</b>	<b>DESCRIPTION OF CHECK</b>
CFh	Test CMOS R/W functionality.
C0h	Early chipset initialization: -Disable shadow RAM -Disable L2 cache (socket 7 or below) -Program basic chipset registers
C1h	Detect memory -Auto-detection of DRAM size, type and ECC. -Auto-detection of L2 cache (socket 7 or below)
C3h	Expand compressed BIOS code to DRAM
C5h	Call chipset hook to copy BIOS back to E000 & F000 shadow RAM.
0h1	Expand the Xgroup codes locating in physical address 1000:0
02h	Reserved
03h	Initial Superio_Early_Init switch.
04h	Reserved
05h	1. Blank out screen 2. Clear CMOS error flag
06h	Reserved
07h	1. Clear 8042 interface 2. Initialize 8042 self-test
08h	1. Test special keyboard controller for Winbond 977 series Super I/O chips. 2. Enable keyboard interface.
09h	Reserved
0Ah	1. Disable PS/2 mouse interface (optional). 2. Auto detect ports for keyboard & mouse followed by a port & interface swap (optional). 3. Reset keyboard for Winbond 977 series Super I/O chips.
0Bh	Reserved
0Ch	Reserved

---

0Dh	Reserved
0Eh	Test F00h segment shadow to see whether it is R/W-able or not. If test fails, keep beeping the speaker.
0Fh	Reserved
10h	Auto detect flash type to load appropriate flash R/W codes into the run time area in F000 for ESCD & DMI support.
11h	Reserved
12h	Use walking 1's algorithm to check out interface in CMOS circuitry. Also set real-time clock power status, and then check for override.
13h	Reserved
14h	Program chipset default values into chipset. Chipset default values are MODBINable by OEM customers.
15h	Reserved
16h	Initial onboard clock generator if Early_Init_Onboard_Generator is defined. See also POST 26h.
17h	Reserved
18h	Detect CPU information including brand, SMI type (Cyrix or Intel) and CPU level (586 or 686).
19h	Reserved
1Ah	Reserved
1Bh	Initial interrupts vector table. If no special specified, all H/W interrupts are directed to SPURIOUS_INT_HDLR & S/W interrupts to SPURIOUS_soft_HDLR.
1Ch	Reserved
1Dh	Initial EARLY_PM_INIT switch.
1Eh	Reserved
1Fh	Load keyboard matrix (notebook platform)
20h	Reserved
21h	HPM initialization (notebook platform)
22h	Reserved
23h	1. Check validity of RTC value: e.g. a value of 5Ah is an invalid value for RTC minute. 2. Load CMOS settings into BIOS stack. If CMOS checksum fails, use default value instead.
24h	Prepare BIOS resource map for PCI & PnP use. If ESCD is valid, take into consideration of the ESCD's legacy information.

---

25h	Early PCI Initialization: -Enumerate PCI bus number. -Assign memory & I/O resource -Search for a valid VGA device & VGA BIOS, and put it into C000:0
26h	1. If Early_Init_Onboard_Generator is not defined Onboard clock generator initialization. Disable respective clock resource to empty PCI & DIMM slots. 2. Init onboard PWM 3. Init onboard H/W monitor devices
27h	Initialize INT 09 buffer
28h	Reserved
29h	1. Program CPU internal MTRR (P6 & PII) for 0-640K memory address. 2. Initialize the APIC for Pentium class CPU. 3. Program early chipset according to CMOS setup. Example: onboard IDE controller. 4. Measure CPU speed.
2Ah	Reserved
2Bh	Invoke Video BIOS
2Ch	Reserved
2Dh	1. Initialize double-byte language font (Optional) 2. Put information on screen display, including Award title, CPU type, CPU speed, full screen logo.
2Eh	Reserved
2Fh	Reserved
30h	Reserved
31h	Reserved
32h	Reserved
33h	Reset keyboard if Early_Reset_KB is defined e.g. Winbond 977 series Super I/O chips. See also POST 63h.
34h	Reserved
35h	Test DMA Channel 0
36h	Reserved
37h	Test DMA Channel 1.
38h	Reserved
39h	Test DMA page registers.
3Ah	Reserved
3Bh	Reserved

---

3Ch	Test 8254
3Dh	Reserved
3Eh	Test 8259 interrupt mask bits for channel 1.
3Fh	Reserved
40h	Test 8259 interrupt mask bits for channel 2.
41h	Reserved
42h	Reserved
43h	Test 8259 functionality.
44h	Reserved
45h	Reserved
46h	Reserved
47h	Initialize EISA slot
48h	Reserved
49h	<ol style="list-style-type: none"> <li>1. Calculate total memory by testing the last double word of each 64K page.</li> <li>2. Program write allocation for AMD K5 CPU.</li> </ol>
4Ah	Reserved
4Bh	Reserved
4Ch	Reserved
4Dh	Reserved
4Eh	<ol style="list-style-type: none"> <li>1. Program MTRR of M1 CPU</li> <li>2. Initialize L2 cache for P6 class CPU &amp; program CPU with proper cacheable range.</li> <li>3. Initialize the APIC for P6 class CPU.</li> <li>4. On MP platform, adjust the cacheable range to smaller one in case the cacheable ranges between each CPU are not identical.</li> </ol>
4Fh	Reserved
50h	Initialize USB Keyboard & Mouse.
51h	Reserved
52h	Test all memory (clear all extended memory to 0)
53h	Clear password according to H/W jumper (Optional)
54h	Reserved
55h	Display number of processors (multi-processor platform)
56h	Reserved

---

57h	1. Display PnP logo 2. Early ISA PnP initialization -Assign CSN to every ISA PnP device.
58h	Reserved
59h	Initialize the combined Trend Anti-Virus code.
5Ah	Reserved
5Bh	(Optional Feature) Show message for entering AWDFLASH.EXE from FDD (optional)
5Ch	Reserved
5Dh	1. Initialize Init_Onboard_Super_IO 2. Initialize Init_Onboard_AUDIO.
5Eh	Reserved
5Fh	Reserved
60h	Okay to enter Setup utility; i.e. not until this POST stage can users enter the CMOS setup utility.
61h	Reserved
62h	Reserved
63h	Reset keyboard if Early_Reset_KB is not defined.
64h	Reserved
65h	Initialize PS/2 Mouse
66h	Reserved
67h	Prepare memory size information for function call: INT 15h ax=E820h
68h	Reserved
69h	Turn on L2 cache
6Ah	Reserved
6Bh	Program chipset registers according to items described in Setup & Auto-configuration table.
6Ch	Reserved
6Dh	1. Assign resources to all ISA PnP devices. 2. Auto assign ports to onboard COM ports if the corresponding item in Setup is set to "AUTO".
6Eh	Reserved
6Fh	1. Initialize floppy controller 2. Set up floppy related fields in 40:hardware.
70h	Reserved

---

71h	Reserved
72h	Reserved
73h	(Reserved
74h	Reserved
75h	Detect & install all IDE devices: HDD, LS120, ZIP, CDROM....
76h	(Optional Feature) Enter AWDFLASH.EXE if: -AWDFLASH.EXE is found in floppy drive. -ALT+F2 is pressed.
77h	Detect serial ports & parallel ports.
78h	Reserved
79h	Reserved
7Ah	Detect & install co-processor
7Bh	Reserved
7Ch	Init HDD write protect.
7Dh	Reserved
7Eh	Reserved
7Fh	Switch back to text mode if full screen logo is supported. - If errors occur, report errors & wait for keys - If no errors occur or F1 key is pressed to continue : wClear EPA or customization logo.
80h	Reserved
81h	Reserved

#### **E8POST.ASM starts**

82h	1. Call chipset power management hook. 2. Recover the text font used by EPA logo (not for full screen logo) 3. If password is set, ask for password.
83h	Save all data in stack back to CMOS
84h	Initialize ISA PnP boot devices
85h	1. USB final Initialization 2. Switch screen back to text mode
86h	Reserved
87h	NET PC: Build SYSID Structure.
88h	Reserved

---

89h	<ol style="list-style-type: none"> <li>1. Assign IRQs to PCI devices</li> <li>2. Set up ACPI table at top of the memory.</li> </ol>
8Ah	Reserved
8Bh	<ol style="list-style-type: none"> <li>1. Invoke all ISA adapter ROMs</li> <li>2. Invoke all PCI ROMs (except VGA)</li> </ol>
8Ch	Reserved
8Dh	<ol style="list-style-type: none"> <li>1. Enable/Disable Parity Check according to CMOS setup</li> <li>2. APM Initialization</li> </ol>
8Eh	Reserved
8Fh	Clear noise of IRQs
90h	Reserved
91h	Reserved
92h	Reserved
93h	Read HDD boot sector information for Trend Anti-Virus code
94h	<ol style="list-style-type: none"> <li>1. Enable L2 cache</li> <li>2. Program Daylight Saving</li> <li>3. Program boot up speed</li> <li>4. Chipset final initialization.</li> <li>5. Power management final initialization</li> <li>6. Clear screen &amp; display summary table</li> <li>7. Program K6 write allocation</li> <li>8. Program P6 class write combining</li> </ol>
95h	Update keyboard LED & typematic rate
96h	<ol style="list-style-type: none"> <li>1. Build MP table</li> <li>2. Build &amp; update ESCD</li> <li>3. Set CMOS century to 20h or 19h</li> <li>4. Load CMOS time into DOS timer tick</li> <li>5. Build MSIRQ routing table.</li> </ol>
FFh	Boot attempt (INT 19h)

---

## Howto : Flash the BIOS

To flash your BIOS you'll need

- 1) a xxxxx.bin file that is a file image of the new BIOS
- 2) AWDFLASH.EXE a utility that can write the data-file into the BIOS chip.

Create a new, clean DOS 6 bootable floppy with "format a: /s".

Copy flash utility and the BIOS image file to this disk.

Turn your computer off. Insert the floppy you just created and boot the computer. As it boots up, hit the [DEL] key to enter the CMOS setup. Go to "LOAD SETUP (or BIOS) DEFAULTS," and then save and exit the setup program. Continue to boot with the floppy disk.

Type "AWDFLASH" to execute the flash utility. When prompted, enter the name of the new BIOS image and begin the flash procedure. Note: If you reboot now, you may not be able to boot again.

After the flash utility is complete, reboot the system.

### ***What to do when the Award flasher says: Insufficient memory***

1. In CMOS Chipset Features Setup, Disable Video Bios Cacheable.
2. Hit Esc, F10, Save and exit.
3. Flash the BIOS and reboot
4. Enter CMOS Chipset Features Setup, and Enable Video Bios Cacheable, hit Esc, F10, Save and reboot.

---

## What if things go wrong

if you use the wrong Flash BIOS or if the writing process gets interrupted, there is a fat chance that your computer won't boot anymore.

### ***How can you recover a corrupt BIOS ?***

**Boot-block booting** (this works only for Award BIOS)

Modern motherboards based on Award BIOS have a boot-block BIOS. This is small area of the BIOS that doesn't get overwritten when you flash a BIOS. The boot-block BIOS only has support for the floppy drive. If you have the AGP video enabled you won't see anything on the screen because the boot-block BIOS only supports an ISA videocard.

If you do not want to change your AGP video setting than proceed as follows:

The boot-block BIOS will execute an AUTOEXEC.BAT file on a bootable diskette. Copy an Award flasher & the correct BIOS \*.bin file on the floppy and execute it automatically by putting awdfash \*.bin in the AUTOEXEC.BAT file.

#### **Solution 2: Hot-swapping**

1. Replace the corrupt chip by a working one. The working BIOS doesn't have to be written for your board, it just has to give you a chance of booting to DOS.

BIOSs for the same chipset mostly work. (Chipsets that not differ too much also mostly work. (e.g. Triton FX chipset and Triton HX chipset)

2. Boot the system to DOS (with floppy or HD)

3. Be sure that the System BIOS cacheable option in your BIOS is enabled! If so replace (while the computer is powered on) the BIOS chip with the corrupt one. This should work fine with most boards because the BIOS is shadowed in RAM.

4. Flash an appropriate BIOS to the corrupt chip and reboot.

**NOTE:** Use a flasher from MRBIOS (<http://www.mrbios.com>). Utilities that come with your motherboard often use specific BIOS-hooks. Because you have booted with a BIOS not written for your motherboard they usually don't work. The MR Flash utilities communicate directly with your Flash Rom and always work. In most cases they flash a non-MRBIOS to your BIOS chip without problems.

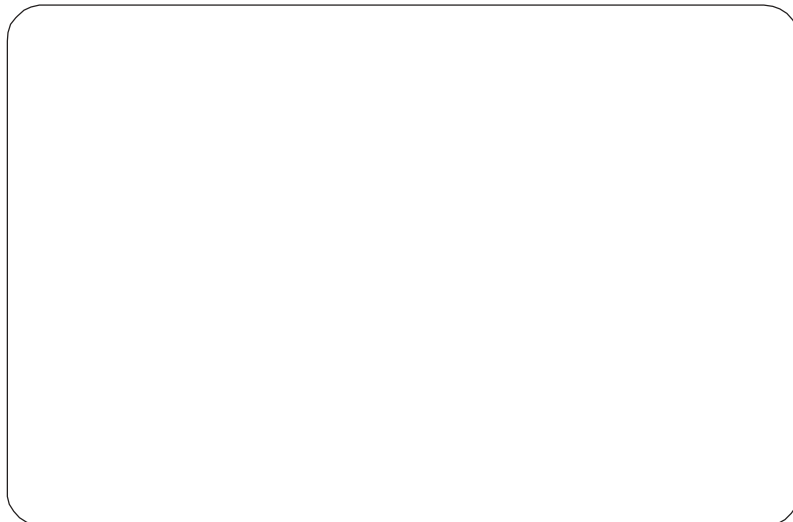
---

## Warranty

This product is warranted to be in good working order for a period of one year from the date of purchase. Should this product fail to be in good working order at any time during this period, we will, at our option, replace or repair it at no additional charge except as set forth in the following terms. This warranty does not apply to products damaged by misuse, modifications, accident or disaster.

Vendor assumes no liability for any damages, lost profits, lost savings or any other incidental or consequential damage resulting from the use, misuse of, or inability to use this product. Vendor will not be liable for any claim made by any other related party.

Return authorization must be obtained from the vendor before returned merchandise will be accepted. Authorization can be obtained by calling or faxing the vendor and requesting a Return Merchandise Authorization (RMA) number. Returned goods should always be accompanied by a clear problem description.



Any advice or comments about our products and service, or anything we can help you with please don't hesitate to contact with us. We will do our best to support you for your products, projects and business

**Global American Inc.**

---

Address	17 Hampshire Drive Hudson, NH 03051
TEL	Toll Free (U.S. Only) 800-833-8999 (603)886-3900
FAX	(603)886-4545
Website	<a href="http://www.globalamericaninc.com">http://www.globalamericaninc.com</a>
E-Mail	<a href="mailto:salesinfo@globalamericaninc.com">salesinfo@globalamericaninc.com</a>

---

