



integration with integrity

3308390 User's Manual

5.25" Embedded Board with Socket P

Version 1.0

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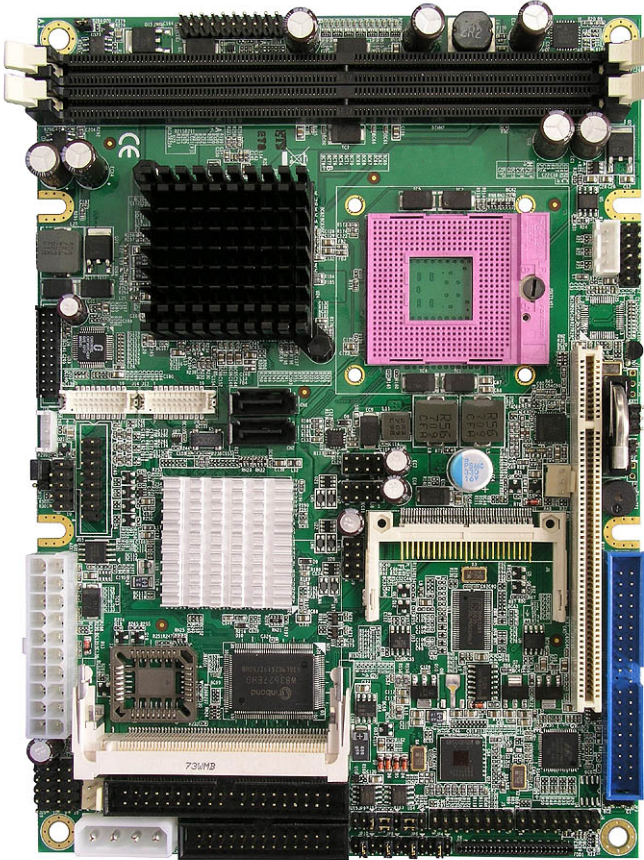
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IMPORTANT NOTE: When the system boots without the CRT being connected, there will be no image on screen when you insert the CRT/VGA cable. To show the image on screen, the hotkey must be pressed (CTRL-ALT-F1).



THE 3308390 5.25" DISK SIZE MOTHERBOARD

Introduction

Product Description

The 3308390 5.25" DISK SIZE board incorporates the Mobile Intel® GME965 series Express Chipset for Embedded Computing, consisting of the Intel® GME965 Graphic Memory Controller Hub (GMCH) and Intel® I/O Controller Hub (ICH8-M), an optimized integrated graphics solution with a 533MHz and 800MHz front-side bus. Dimensions of the board are 203mm x 146mm.

The integrated powerful 3D graphics engine, based on Intel® Graphics Media Accelerator X3100 (Intel® GMA X3100) architecture, operates at core speeds of up to 400 MHz. It features a low-power design, is validated with the Intel® Core 2 Duo and Intel® Celeron processors on 65nm process. With dual channel DDR2 667MHz two DIMM socket on board, the board supports up to 4GB of DDR2 system memory.

Intel® Graphics supports a unique intelligent memory management scheme called Dynamic Video Memory Technology (DVMT). DVMT handles diverse applications by providing the maximum (384MB) availability of system memory for general computer usage, while supplying additional graphics memory when a 3D-intensive application requests it. The Intel GMA X3100 graphics architecture also takes advantage of the high-performance Intel processor. Intel GMA X3100 graphics supports Dual Independent Display technology.

The main features of the board are:

- Supports Intel® Core™ 2 Duo (Merom 800MHz), Intel® Celeron
- Supports up to 2.4GHz, 533MHz/800MHz FSB
- Two DDR2 SDRAM DIMM, Max. 4GB memory
- Onboard Intel Gigabit LAN and Marvell PCI-Express Gigabit LAN
- Intel® GME965 Express VGA for CRT / LVDS
- 2x SATA, 6x USB 2.0, 4x COM, Watchdog timer
- 1x MiniPCI, 1x PCI, 1 DVI (connector on cable)

Checklist

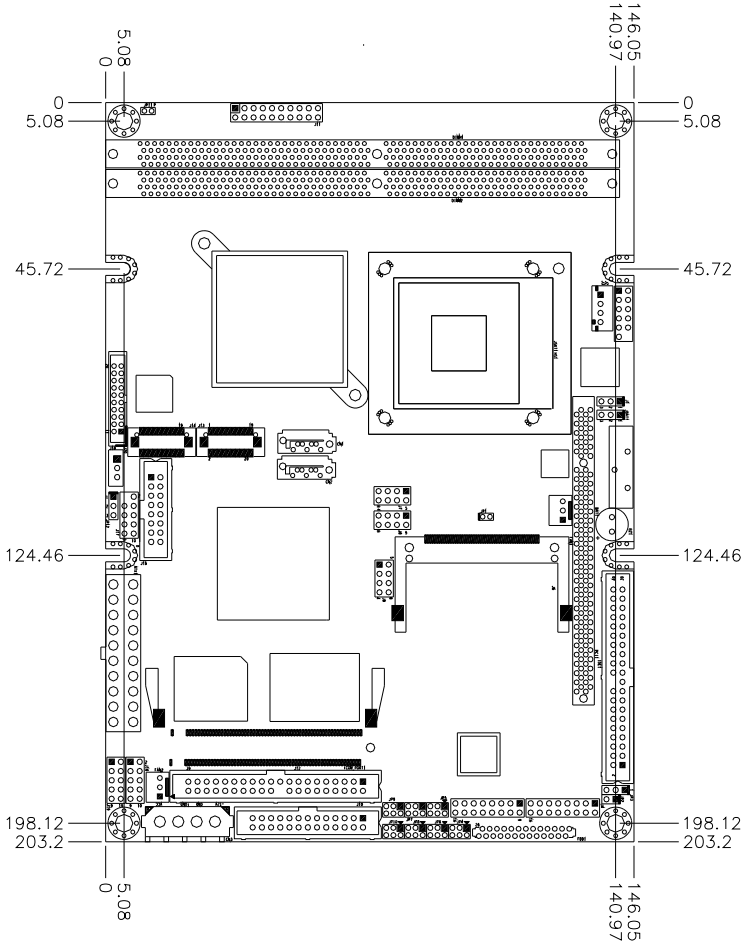
Your 3308390 package should include the items listed below.

- The 3308390 5.25" disk-size motherboard
- This User's Manual
- 1 CD containing chipset drivers and flash memory utility
- Options:
 - Cable kit
 - Dual RJ-45 connector board

3308390 Specifications

CPU Supported	Intel® Core™ 2 Duo, Intel Celeron mobile processors
CPU Voltage	0.700V ~ 1.5V (IMVP-6)
System Speed	Up to 2.4GHz or above
CPU FSB	533MHz/800MHz FSB
Cache	1MB/2MB/4MB
Green /APM	APM1.2
CPU Socket	mPGA Socket 478
Chipset	Intel GME965 Chipset GMCH: GME965 1299-pin Micro-FCBGA ICH8M: 82801HBM 676-pin mBGA
BIOS	Award BIOS, support ACPI Function
Memory	DDR2 667/533 SDRAM DIMM x2 (w/o ECC), Max. 4GB
VGA	Built-in, supports CRT
SDVO	Built-in Chronitel 7307C, DVI port)
LVDS LCD Panel	GME965 built-in, supports 24+24 bits (Type 1 only), single or dual channel LVDS
LAN	1. ICH8M 10/100/gigabit MAC + PHY: <ul style="list-style-type: none"> • Intel 82566DM Nineveh 10/100/1000 2. Marvell 88E8053 PCI-e Gigabit LAN controller x1
USB	ICH8M built-in USB 2.0 host controller, support 6 ports
Serial ATA Ports	ICH8M built-in SATA controller, supports 2 ports
Parallel IDE	ICH8M built-in one channel Ultra DMA 33/66/100, CF Type II
Audio	ICH8M Built-in High Definition audio Codec ALC885
LPC I/O	W83627EHF: COM1, COM2 (RS232/RS422/RS485), parallel port x1, slim FDC 1.44MB, hardware monitor (3 thermal, 4 voltage monitor inputs, 2 fan headers) Fintek F81216D: COM3, COM4
Digital IO	4 in & 4 out
Keyboard/Mouse	Supports PS/2 Keyboard/Mouse Connector
Expansion Slots	PCI slot x1, Mini PCI socket x1
Onboard Header/Connector	Pin headers for: PS/2 keyboard/mouse, two Gigabit LAN1, 2, COM1~4, audio Line-Out, Line-In & Mic, CD in IDE1, slim floppy, parallel port, Digital I/O, USB1~6, DVI, VGA CRT Connectors for: SATA ports, CF type II Connector, LVDS
Watchdog Timer	Yes (256 segments, 0, 1, 2...255 sec/min)
System Voltage	+5V, +3.3V, +12V, -12V, 5VSB (2A)
Others	Modem Wakeup, LAN Wakeup
Board Size	203mm x 146mm (5.25" DISK SIZE)

Board Dimensions



Installations

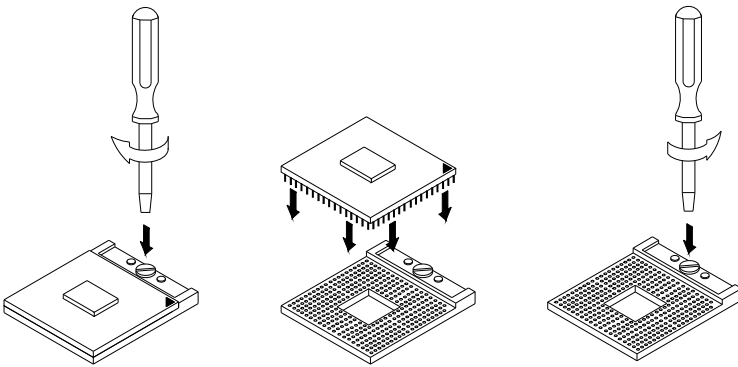
This section provides information on how to use the jumpers and connectors on the 3308390 in order to set up a workable system. The topics covered are:

Installing the CPU	6
Installing the Memory	7
Setting the Jumpers.....	8
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Installing the CPU

The 3308390 board supports a Socket 478MN (MEROM) processor socket for Intel® Core™ 2 Duo, Intel® Celeron mobile processors.

The processor socket comes with a screw to secure the processor. As shown in the left picture below, loosen the screw first before inserting the processor. Place the processor into the socket by making sure the notch on the corner of the CPU corresponds with the notch on the inside of the socket. Once the processor has slide into the socket, fasten the screw. Refer to the figures below.



NOTE: *Ensure that the CPU heat sink and the CPU top surface are in total contact to avoid CPU overheating problem that would cause your system to hang or be unstable.*

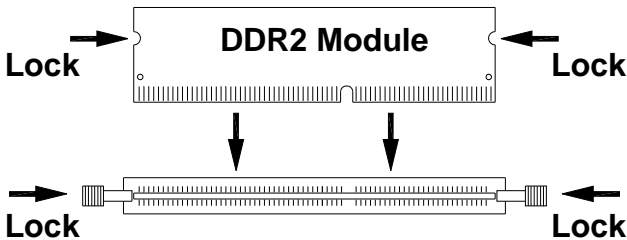
Installing the Memory

The 3308390 board supports two DDR2 memory socket for a maximum total memory of 4GB in DDR2 memory type.

Installing and Removing Memory Modules

To install the DDR2 modules, locate the memory slot on the board and perform the following steps:

1. Hold the DDR2 module so that the key of the DDR2 module aligned with that on the memory slot.
2. Gently push the DDR2 module in an upright position until the clips of the slot close to hold the DDR2 module in place when the DDR2 module touches the bottom of the slot.
3. To remove the DDR2 module, press the clips with both hands.



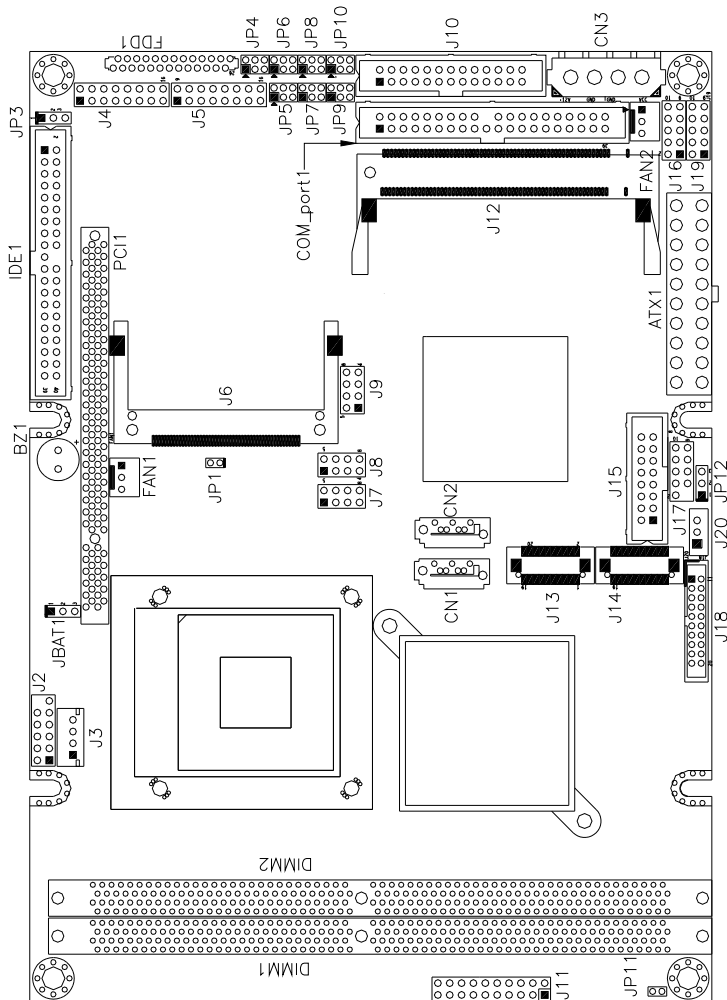
Setting the Jumpers

Jumpers are used on 3308390 to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on 3308390 and their respective functions.

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JBAT1: Clear CMOS Setting.....	10
JP1: CompactFlash Slave/Master Selection.....	10
JP3: PCI Riser Card Selection	10
JP4, JP6, JP8, JP10: Serial Port RI_pin V-out Selection	10
JP5, JP7, JP9: RS232/422/485 (COM2) Selection	11
JP11: AT/ATX power on type Selection	11
JP12: LCD Panel Power Selection.....	11



IMPORTANT NOTE: When the system boots without the CRT being connected, there will be no image on screen when you insert the CRT/VGA cable. To show the image on screen, the hotkey (CTRL-ALT-F1) must be pressed.

Jumper Locations on 3308390





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

JBAT1: Clear CMOS Setting

JBAT1	Setting
	Normal
	Clear CMOS

JP1: CompactFlash Slave/Master Selection

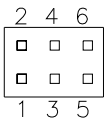
JP1	CF Setting
	Master
	Slave

JP3: PCI Riser Card Selection

JP3	Riser Card
	One PCI bus master
	Two PCI bus masters

JP4, JP6, JP8, JP10: Serial Port RI_pin V-out Selection

The following table describes the jumper settings for COM port selection.



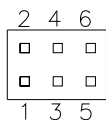
COM Function	12V	RI	5V
JP4 (COM1)	1-2	3-4	5-6
JP6 (COM2)	1-2	3-4	5-6
JP8 (COM3)	1-2	3-4	5-6
JP10 (COM4)	1-2	3-4	5-6

JP5, JP7, JP9: RS232/422/485 (COM2) Selection

COM1, COM3, COM4 are fixed for RS-232 use only.

COM2 is selectable for RS232, RS-422 and RS-485.

The following table describes the jumper settings for COM2 selection.



COM2 Function	RS-232	RS-422	RS-485
Jumper Setting (pin closed)	JP9: 1-2	JP9: 3-4	JP9: 5-6
	JP7: 3-5 & 4-6	JP7: 1-3 & 2-4	JP7: 1-3 & 2-4
	JP5: 3-5 & 4-6	JP5: 1-3 & 2-4	JP5: 1-3 & 2-4

JP11: AT/ATX power on type Selection

JP1	Power on type
 Short	Auto power on (delay 5 seconds)
 Open	Push power on button

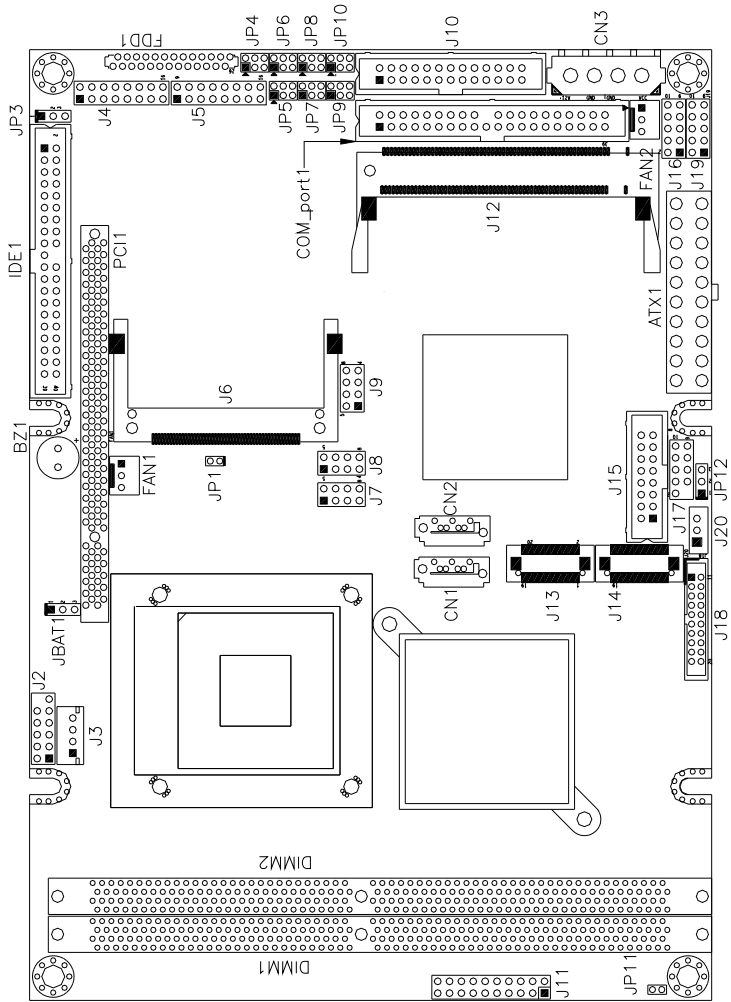
JP12: LCD Panel Power Selection

JP12	LCD Panel Power
 1 2 3	3.3V
 1 2 3	5V

Connectors on 3308390

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J15: VGA Connector	20
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Connector Locations on 3308390



FAN1: CPU Fan Power Connector

FAN1 is a 3-pin header for CPU fans. The fan must be a 12V.



Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection

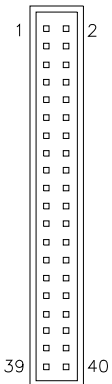
FAN2: System Fan Power Connector

FAN2 is a 3-pin header for the system fan. The fan must be a 12V fan (500mA).



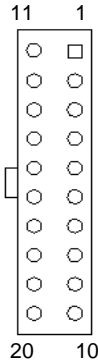
Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection

IDE1: IDE Connector



Signal Name	Pin #	Pin #	Signal Name
Reset IDE	1	2	Ground
Host data 7	3	4	Host data 8
Host data 6	5	6	Host data 9
Host data 5	7	8	Host data 10
Host data 4	9	10	Host data 11
Host data 3	11	12	Host data 12
Host data 2	13	14	Host data 13
Host data 1	15	16	Host data 14
Host data 0	17	18	Host data 15
Ground	19	20	Protect pin
DRQ0	21	22	Ground
Host IOW	23	24	Ground
Host IOR	25	26	Ground
IOCHRDY	27	28	Host ALE
DACK0	29	30	Ground
IRQ14	31	32	No connect
Address 1	33	34	No connect
Address 0	35	36	Address 2
Chip select 0	37	38	Chip select 1
Activity	39	40	Ground

ATX1: ATX Power Supply Connector



Signal Name	Pin #	Pin #	Signal Name
3.3V	11	1	3.3V
-12V	12	2	3.3V
Ground	13	3	Ground
PS-ON	14	4	+5V
Ground	15	5	Ground
Ground	16	6	+5V
Ground	17	7	Ground
-5V	18	8	Power good
+5V	19	9	5VSB
+5V	20	10	+12V

COM_PORT: COM1~COM4 Serial Ports Connector



Pin #	Signal Name (RS-232)
1	DCD, Data carrier detect
2	RXD, Receive data
3	TXD, Transmit data
4	DTR, Data terminal ready
5	Ground
6	DSR, Data set ready
7	RTS, Request to send
8	CTS, Clear to send
9	RI, Ring indicator
10	No Connect.

CN1, CN2: SATA Connectors

CN3: 5V & 12V output Connector



Pin #	Signal Name
1	12V
2	Ground
3	Ground
4	5V

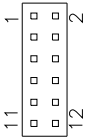
FDD1: Floppy Drive Connector

FDD1 is a slim 26-pin connector and will support up to 2.88MB FDD.



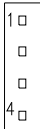
Signal Name	Pin #	Pin #	Signal Name
VCC	1	2	INDEX
VCC	3	4	DRV_SEL
VCC	5	6	DSK_CH
NC	7	8	NC
NC	9	10	MOTOR
DINST	11	12	DIR
NC	13	14	STEP
GND	15	16	WDATA
GND	17	18	WGATE
GND	19	20	TRACK
NC	21	22	WPROT
GND	23	24	RDATA
GND	25	26	SIDE

J2: Audio Connector



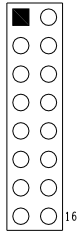
Signal Name	Pin #	Pin #	Signal Name
LINEOUT R	1	2	LINEOUT L
Ground	3	4	Ground
LINEIN R	5	6	LINEIN L
Ground	7	8	Ground
Mic-In	9	10	VREFOUT
Ground	11	12	Protect pin

J3: CD-In Pin Header



Pin #	Signal Name
1	CD Audio L
2	Ground
3	Ground
4	CD Audio R

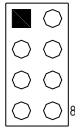
J4, J5: Gbe RJ-45 Connector



Signal Name	Pin #	Pin #	Signal Name
MIDP0	1	9	MIDN0
V2.5	2	10	GND
MIDP1	3	11	MIDN1
MIDP2	4	12	MIDN2
N.C.	5	13	GND
MIDP3	6	14	MIDN3
LED1+	7	15	LED1-
LED2+	8	16	LED2-

J6: Compact Flash Connector

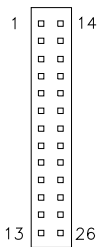
J7, J8, J9: USB Connectors



Signal Name	Pin	Pin	Signal Name
Vcc	1	5	Ground
D0-	2	6	D1+
D0+	3	7	D1-
Ground	4	8	Vcc

J10: Parallel Port Connector

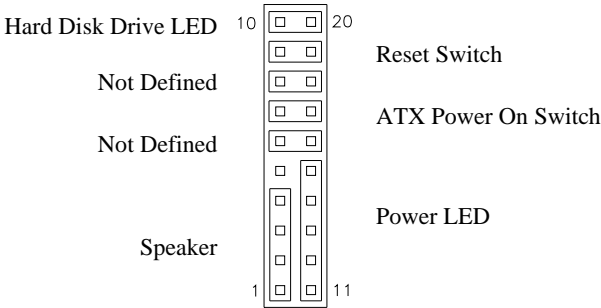
The following table describes the pin out assignments of this connector.



Signal Name	Pin #	Pin #	Signal Name
Line printer strobe	1	14	AutoFeed
PD0, parallel data 0	2	15	Error
PD1, parallel data 1	3	16	Initialize
PD2, parallel data 2	4	17	Select
PD3, parallel data 3	5	18	Ground
PD4, parallel data 4	6	19	Ground
PD5, parallel data 5	7	20	Ground
PD6, parallel data 6	8	21	Ground
PD7, parallel data 7	9	22	Ground
ACK, acknowledge	10	23	Ground
Busy	11	24	Ground
Paper empty	12	25	Ground
Select	13	N/A	N/A

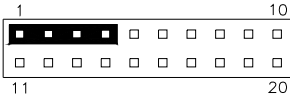
J11 (F_PANEL): System Function Connector

J11 provides connectors for system indicators that provide light indication of the computer activities and switches to change the computer status. J11 is a 20-pin header that provides interfaces for the following functions.



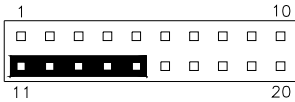
Speaker: Pins 1 - 4

This connector provides an interface to a speaker for audio tone generation. An 8-ohm speaker is recommended.



Pin #	Signal Name
1	Speaker out
2	No connect
3	Ground
4	+5V

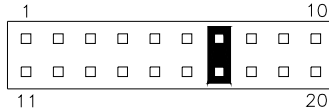
Power LED: Pins 11 - 15



Pin #	Signal Name
11	Power LED
12	No connect
13	Ground
14	No connect
15	Ground

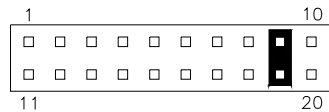
ATX Power ON Switch: Pins 7 and 17

This 2-pin connector is an “ATX Power Supply On/Off Switch” on the system that connects to the power switch on the case. When pressed, the power switch will force the system to power on. When pressed again, it will force the system to power off.



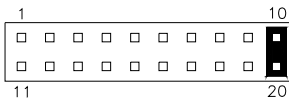
Reset Switch: Pins 9 and 19

The reset switch allows the user to reset the system without turning the main power switch off and then on again. Orientation is not required when making a connection to this header.



Hard Disk Drive LED Connector: Pins 10 and 20

This connector connects to the hard drive activity LED on control panel. This LED will flash when the HDD is being accessed.

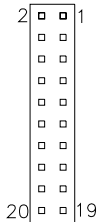


Pin #	Signal Name
10	HDD Active
20	5V

J12: Mini PCI Connector

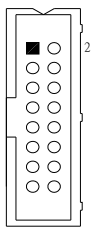
J14, J13: LVDS Connectors (1st channel, 2nd channel)

The LVDS connectors on board consist of the first channel (J14) and second channel (J13) and supports 18-bit or 24-bit.



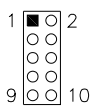
Signal Name	Pin #	Pin #	Signal Name
TX0-	2	1	TX0+
Ground	4	3	Ground
TX1-	6	5	TX1+
5V/3.3V	8	7	Ground
TX3-	10	9	TX3+
TX2-	12	11	TX2+
Ground	14	13	Ground
TXC-	16	15	TXC+
5V/3.3V	18	17	ENABKL
+12V	20	19	+12V

J15: VGA Connector



Signal Name	Pin #	Pin #	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
5V	9	10	GND
N.C.	11	12	DDC_data
HSYNC	13	14	VSYNC
DDC_clk	15		

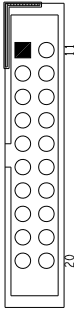
J16: Digital I/O



Signal Name	Pin #	Pin #	Signal Name
GND	1	2	VCC
OUT3	3	4	OUT1
OUT2	5	6	OUT0
IN3	7	8	IN1
IN2	9	10	IN0

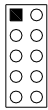
J17: SPI Flash Connector (factory use only)

J18: DVI Port Connector



Signal Name	Pin #	Pin #	Signal Name
TX1+	1	11	TX2+
TX1-	2	12	TX2-
GND	3	13	GND
GND	4	14	GND
TXCK+	5	15	TX0+
TXCK-	6	16	TX0-
GND	7	17	N.C.
+5V	8	18	N.C.
DVI-DET	9	19	DDC_DATA
N.C.	10	20	DDC_CLK

J19: PS/2 Keyboard and PS/2 Mouse Connectors



Signal Name	Pin #	Pin #	Signal Name
GND	1	2	GND
5V	3	4	5V
Mouse data	5	6	Keyboard data
Mouse clock	7	8	Keyboard clock
N.C.	9	10	N.C.

J20: LCD Backlight Connector



Pin #	Signal Name
1	+12V
2	Backlight Enable
3	Ground

PCI1: PCI Slot (supports 2 Master)

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Appendix

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
1F0h - 1F7h	IDE Interface
278 - 27F	Parallel Port #2(LPT2)
2F8h - 2FFh	Serial Port #2(COM2)
2B0 - 2DF	Graphics adapter Controller
378h - 3FFh	Parallel Port #1(LPT1)
360 - 36F	Network Ports
3B0 - 3BF	Monochrome & Printer adapter
3C0 - 3CF	EGA adapter
3D0 - 3DF	CGA adapter
3F0h - 3F7h	Floppy Disk Controller
3F8h - 3FFh	Serial Port #1(COM1)

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Reserved
IRQ6	Floppy Disk Controller
IRQ7	Parallel Port #1
IRQ8	Real Time Clock
IRQ9	Reserved
IRQ10	Reserved
IRQ11	Reserved
IRQ12	PS/2 Mouse
IRQ13	80287
IRQ14	Primary IDE
IRQ15	Secondary IDE

C. Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

```
//=====
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//=====
#include <stdio.h>
#include <stdlib.h>
#include "W627EHF.H"
//=====
int main (int argc, char *argv[]);
void copyright(void);
void EnableWDT(int);
void DisableWDT(void);
//=====
int main (int argc, char *argv[])
{
    unsigned char bBuf;
    unsigned char bTime;
    char **endptr;

    copyright();

    if (argc != 2)
    {
        printf(" Parameter incorrect!!\n");
        return 1;
    }

    if (Init_W627EHF() == 0)
    {
        printf(" Winbond 83627HF is not detected, program abort.\n");
        return 1;
    }
    bTime = strtol (argv[1], endptr, 10);
    printf("System will reset after %d seconds\n", bTime);

    EnableWDT(bTime);

    return 0;
}
//=====
```

```

void copyright(void)
{
    printf("\n===== Winbond 83627EHF Watch Timer Tester (AUTO DETECT) =====\n")
        " Usage : W627E_WD reset_time\n"
        " Ex : W627E_WD 3 => reset system after 3 second\n"
        " W627E_WD 0 => disable watch dog timer\n");
}
//=====
void EnableWDT(int interval)
{
    unsigned char bBuf;

    bBuf = Get_W627EHF_Reg( 0x2D);
    bBuf &= (!0x01);
    Set_W627EHF_Reg( 0x2D, bBuf); //Enable WDTO

    Set_W627EHF_LD( 0x08); //switch to logic device 8
    Set_W627EHF_Reg( 0x30, 0x01); //enable timer

    bBuf = Get_W627EHF_Reg( 0xF5);
    bBuf &= (!0x08);
    Set_W627EHF_Reg( 0xF5, bBuf); //count mode is second

    Set_W627EHF_Reg( 0xF6, interval); //set timer
}
//=====
void DisableWDT(void)
{
    Set_W627EHF_LD(0x08); //switch to logic device 8
    Set_W627EHF_Reg(0xF6, 0x00); //clear watchdog timer
    Set_W627EHF_Reg(0x30, 0x00); //watchdog disabled
}
//=====

```

```

//=====
//
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// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//=====
#include "W627EHF.H"
#include <dos.h>
//=====
unsigned int W627EHF_BASE;
void Unlock_W627EHF (void);
void Lock_W627EHF (void);
//=====
unsigned int Init_W627EHF(void)
{
    unsigned int result;
    unsigned char ucDid;

    W627EHF_BASE = 0x2E;
    result = W627EHF_BASE;

    ucDid = Get_W627EHF_Reg(0x20);
    if (ucDid == 0x88)
    {
        goto Init_Finish;
    }

    W627EHF_BASE = 0x4E;
    result = W627EHF_BASE;
    ucDid = Get_W627EHF_Reg(0x20);
    if (ucDid == 0x88)
    {
        goto Init_Finish;
    }

    W627EHF_BASE = 0x00;
    result = W627EHF_BASE;
}

Init_Finish:
    return (result);
}
//=====
void Unlock_W627EHF (void)
{
    outportb(W627EHF_INDEX_PORT, W627EHF_UNLOCK);
    outportb(W627EHF_INDEX_PORT, W627EHF_UNLOCK);
}
//=====
void Lock_W627EHF (void)
{
    outportb(W627EHF_INDEX_PORT, W627EHF_LOCK);
}
//=====
void Set_W627EHF_LD( unsigned char LD)
{
    Unlock_W627EHF();
    outportb(W627EHF_INDEX_PORT, W627EHF_REG_LD);
    outportb(W627EHF_DATA_PORT, LD);
    Lock_W627EHF();
}

```

```

=====
void Set_W627EHF_Reg( unsigned char REG, unsigned char DATA)
{
    Unlock_W627EHF();
    outportb(W627EHF_INDEX_PORT, REG);
    outportb(W627EHF_DATA_PORT, DATA);
    Lock_W627EHF();
}
=====
unsigned char Get_W627EHF_Reg(unsigned char REG)
{
    unsigned char Result;
    Unlock_W627EHF();
    outportb(W627EHF_INDEX_PORT, REG);
    Result = inportb(W627EHF_DATA_PORT);
    Lock_W627EHF();
    return Result;
}
=====

=====
//
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// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
=====
#ifndef __W627EHF_H
#define __W627EHF_H                1
=====
#define    W627EHF_INDEX_PORT      (W627EHF_BASE)
#define    W627EHF_DATA_PORT      (W627EHF_BASE+1)
=====
#define    W627EHF_REG_LD          0x07
=====
#define W627EHF_UNLOCK              0x87
#define    W627EHF_LOCK            0xAA
=====
unsigned int Init_W627EHF(void);
void Set_W627EHF_LD( unsigned char);
void Set_W627EHF_Reg( unsigned char, unsigned char);
unsigned char Get_W627EHF_Reg( unsigned char);
=====
#endif //__W627EHF_H

```

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