

# User's Manual

Industrial PC-based Automation

## **3307252**

Half-size ISA-bus Socket 370  
Pentium-III/Celeron PC-133 CPU Card  
with 4xAGP 3D SVGA, Fast Ethernet  
Interface and DiskOnChip Socket

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## Introduction

The 3307252 is based on VIA's ProSavage™ PL133 that combines PC-133, 133MHz FSB, ATA-100 technologies and rich 4xAGP 2D/3D graphics capabilities in a single package. Its onboard 10Base-T/100Base-TX Ethernet, CRT display controller and Panel Link LCD daughterboards add communication and multimedia features to its powerful graphics function.

A wide range of CPUs including Intel® Pentium® III/ Celeron™ and VIA Cyrix® III processors are supported up to 1GHz at 133MHz FSB, while memory is expandable to 512MB at PC-133 SDRAM.

The VIA ProSavage™ PL133 dual-chipset consists of the VT8604 Northbridge and VT82C686B Super Southbridge. It integrates VIA Apollo Pro133A chipset with 4XAGP 32MB S3® Savage4™ and S3® Savage2000™ 2D graphics core.

The highlight of the Super Southbridge is the support for high speed PCI UltraATA/100 enhanced IDE which can tremendously increase transfer speed for database applications. Other exclusive features include DiskOnChip® 2000 socket for memory up to 288MB.

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# Specifications

## General Specifications

- CPU : Socket 370 FC-PGA/PPGA supports : Intel® Pentium®III, Intel® Celeron™, VIA Cyrix® III with FSB @ 133 / 100 / 66 MHz
- Chipset : VIA ProSavage™ PL133 (VT8604 Northbridge and VT82C686B “Super” Southbridge) integrates VIA Apollo Pro133A, S3® Savage4™ 3D and S3® Savage2000™ 2D engines and supports PC-133, 133MHz FSB and UltraATA/100 interfaces.
- BIOS : AWARD Flash BIOS Green&Soft Off function, LS120, Multiple boot function
- Green Function : power saving supported in BIOS. DOZE /STANDBY / SUSPEND modes, ACPI & APM
- Secondary Cache : Integrated on CPU
- DRAM Memory : up to 512MB of SDRAM in one 168-pin DIMM sockets (supports PC-133 SDRAM)
- PCI Enhanced IDE with Ultra DMA : supports 2 ports and up to 4 ATAPI devices. UltraDMA transfer 33/66 and 100 MB/sec, 40-pin box header and 44-pin notebook size box header
- Watchdog Timer : 127-level timer generates RESET or NMI when your application loses control over the system.
- Real-time Clock : built-in chipset with lithium battery backup for 10 years of data retention. CMOS data backup of BIOS setup and BIOS default.

## High Speed Multi I/O

- Chipset : included in VT82C686B “Super” Southbridge
- Serial Ports : one external high speed RS-232C port COM1 (DB9 on bracket), one internal high speed RS-232C/422/485 port COM2 (jumper selectable, 10-pin box header). Both with 16C550 compatible UART and 16 byte FIFO.
- USB : 2 onboard USB ver 1.0 ports (2x 5-pin header)
- SIR Interface : onboard IrDA TX/RX port (5-pin header)
- Floppy Disk Drive Interface : 2 floppy disk drives, 5¼" (360 KB or 1.2 MB) and 3½" (720 KB, 1.44 MB or 2.88 MB).
- Bi-directional Parallel Port : SPP, EPP and ECP mode.
- Keyboard and Mouse Connectors : external PS/2 KB/Mouse port (2-in-1 mini DIN) onboard AT Keyboard port (5-pin box header)

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## Network Interface Controller

- Chipset : Intel 82559, 10/100 Mbps, autoswitching
- Connector : external RJ-45 with LEDs on bracket

## Display Controller

- Chipset : 4x AGP S3® Savage4™ 3D and S3® Savage 2000™ 2D engines integrated in VT8604 Supports up to 32 MB (shared) SDRAM
- Display Type : CRT (VGA, SVGA, XGA, SXGA) LCD (optional, see LCD Daughterboard)
- Connectors : external DB-15 for CRT on bracket and 42-pin header for TMDS LCD Display daughterboard
- LCD Display Daughterboard (optional) : TMDS (Panel Link) with DVI interface and 20-pin connector for LCD monitor

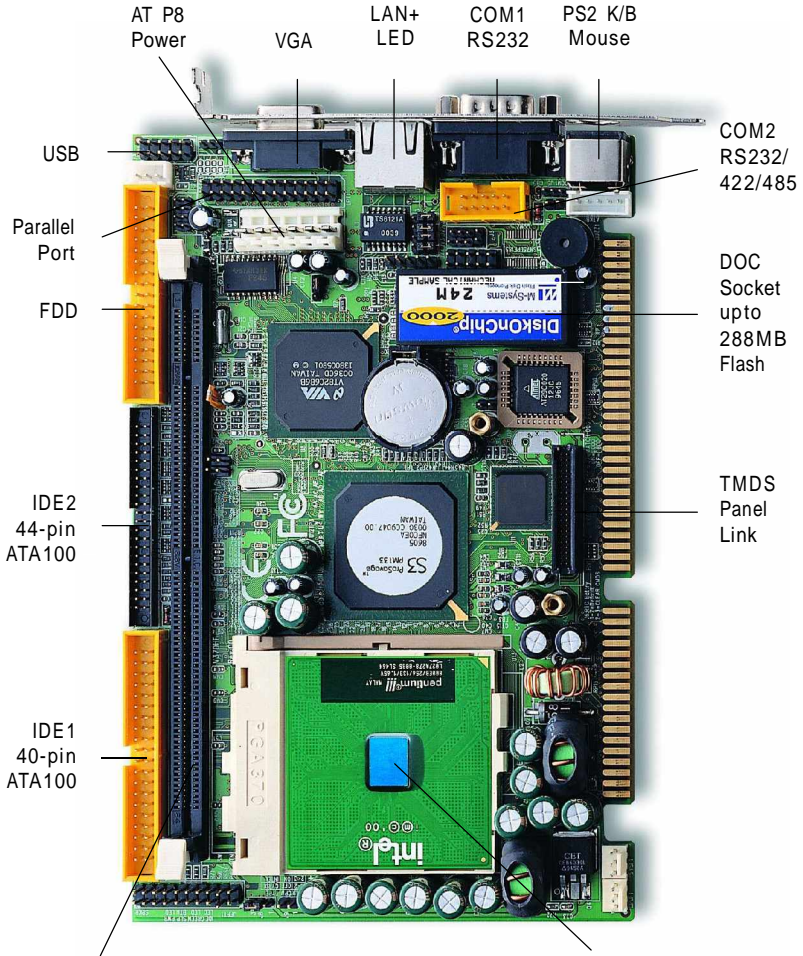
## Flash Disk DiskOnChip®2000

- Package : Single Chip Flash Disk in 32-pin DIP JEDEC
- Capacity : up to 288 MByte
- Data Reliability : ECC/EDC error correction
- memory Window : 8 KByte

## Environmental and Power

- Power Requirements : +5 V @ 4.5 A (typical), ±12 V ; (FC-PGA Pentium III 800 MHz at 133 FSB and 256 MB PC-133 SDRAM)
- CPU Power : onboard PWM switching power supply for autodetects CPU core voltage
- System Monitoring and Alarm : CPU and System temperature, system voltage and cooling fan RPM.
- Board Dimensions : 185 mm x 122 mm
- Board Weight : 0.26 Kg.
- Operating Temperature : 0 to 60°C (32 to 140°F)

# Component Location



One 168-pin DIMM  
Socket upto 512MB  
PC-133 SDRAM

Socket 370 for Intel Pentium-III / Celeron  
and VIA Cyrix-III CPUs upto 1GHz at 66/  
100/133 MHz of FSB

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# Warning

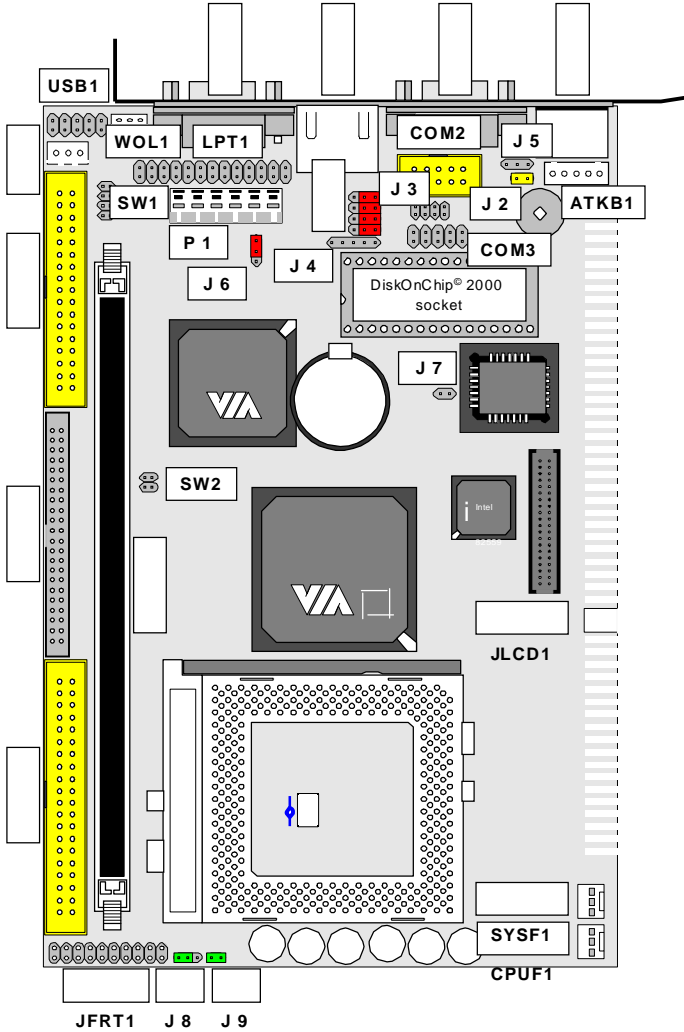
Single Board Computers and their components contain very delicate Integrated Circuits (IC). To protect the Single Board Computer and its components against damage from static electricity, you should always follow the following precautions when handling it :

1. Disconnect your Single Board Computer from the power source when you want to work on the inside
2. Hold the board by the edges and try not to touch the IC chips, leads or circuitry
3. Use a grounded wrist strap when handling computer components.
4. Place components on a grounded antistatic pad or on the bag that came with the Single Board Computer, whenever components are separated from the system

## Ordering Codes

- |         |   |
|---------|---|
| 3307252 | Half-size ISA-bus Socket 370 Pentium-III / Celeron<br>PC-133 CPU Card with 4xAGP 3D SVGA, Fast<br>Ethernet Interface and DiskOnChip® Socket |
| 3901140 | : TMD5 Daughterboard with 20-pin LCD Monitor Cable Kit  |

# Board Layout Front



Jumper Colors	
Green	CPU Speed Ratio
Red	Voltage Settings
Yellow	General Configuration

# Jumper/Connector Quick Reference

## Jumpers

J8/J9 CPU Type Selection

CPU type	J8	J9
Intel PPGA	2-3	OFF
Intel FC-PGA	2-3	ON
VIA C3 (Old)	1-2	OFF

SW1 CPU Clock Ratio

Ratio	7-8	5-6	3-4	1-2
2.0	ON	ON	ON	ON
2.5	ON	OFF	ON	ON
3.0	ON	ON	OFF	ON
3.5	ON	OFF	OFF	ON
4.0	ON	ON	ON	OFF
4.5	ON	OFF	ON	OFF
5.0	ON	ON	OFF	OFF
5.5	ON	OFF	OFF	OFF
6.0	OFF	ON	ON	ON
6.5	OFF	OFF	ON	ON
7.0	OFF	ON	OFF	ON
7.5	OFF	OFF	OFF	ON
8.0	OFF	ON	ON	OFF
Auto	OFF	OFF	OFF	OFF

SW2 FSB Speed Selection FSB

	1-2	3-4	FSB
Auto / 133 MHz	OFF	OFF	OFF
100 MHz		OFF	ON
66 Mhz		ON	ON

J6 CMOS Operation

1-2	->	Normal Operation
2-3	->	Clear CMOS

J7 DiskOnChip Base Address

ON	->	D0000h
OFF	->	D8000h

J5 Watchdog Active Mode

1-2	->	Active NMI
2-3	->	System RESET
OFF	->	Disable

JV1~JV4 COM1(2) RS-232 Mode

	JV1(2)	JV3(4)
Standard	1-2	1-2
POS : 5V	1-2	2-3
POS : 12V	2-3	1-2
POS : 5V and 12V	2-3	2-3

J2 RS-232/422/485 Mode  
COM2 J8

RS-232 on COM2	ON
RS-422/485 on COM3	OFF

J3 RS-422/485 Mode Selection

	1-2	3-4	5-6	7-8
RS-485	on	on	on	on
RS-422				
TX/RX enbld	off	off	off	off
RX RTS, TX enbld	on	off	off	off
TX RTS, RX enbld	off	on	off	off
TX/RX by RTS	on	on	off	off

## Connectors

CPUF1	CPU Fan Power
SYSF1	System Fan Power
JLCD1	Flat Panel Module
COM1	COM 1 on bracket
KB1	PS/2 Mouse / Keyboard
J1	RJ-45 LAN on bracket
VGA1	CRT SVGA on bracket
J4	IrDA Header
ATKB1	internal AT Keyboard
COM2	COM2 in RS-232 mode
COM3	RS422/485 Mode
WOL1	Wake On LAN
ATX1	ATX Signal Connector
FDD1	FDD interface
LPT1	Parallel PORT
IDE1	40-pin IDE
IDE2	44-pin IDE
USB1	Primary/Secondary USB
P1	AT P8 Power Connector
JFRT1	Front Panel Header

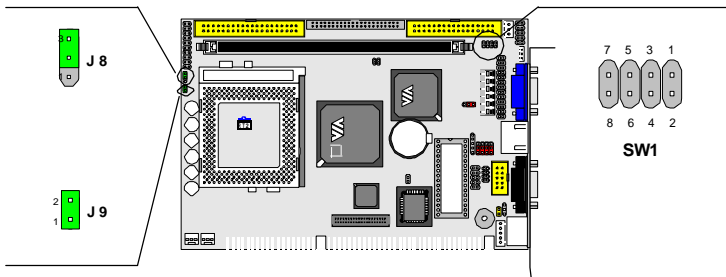
# CPU and CMOS Jumper Settings

## CPU Type Selector

Connector : J8, J9

Type : J8: onboard 3-pin header; J9: onboard 2-pin header

CPU Type	J8	J9
Intel PPGA Celeron	2-3	OFF
Intel FC-PGA Pentium III / Celeron, VIA C3 Ezra / Matthew	2-3	ON
VIA C3 Joshua / Samuel 1/2	1-2	OFF
default setting		



## CPU Host Clock Ratio Selector

Connector : SW1

Type : onboard 8-pin header

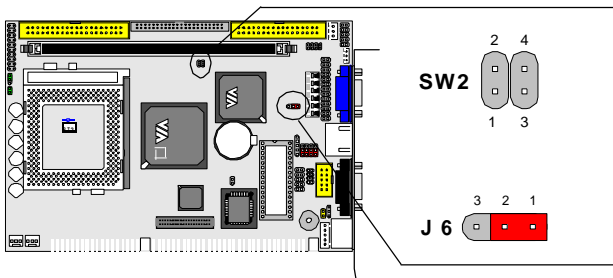
Ratio	SW1			
	7-8	5-6	3-4	1-2
2.0	ON	ON	ON	ON
2.5	ON	OFF	ON	ON
3.0	ON	ON	OFF	ON
3.5	ON	OFF	OFF	ON
4.0	ON	ON	ON	OFF
4.5	ON	OFF	ON	OFF
5.0	ON	ON	OFF	OFF
5.5	ON	OFF	OFF	OFF
6.0	OFF	ON	ON	ON
6.5	OFF	OFF	ON	ON
7.0	OFF	ON	OFF	ON
7.5	OFF	OFF	OFF	ON
8.0	OFF	ON	ON	OFF
Auto	OFF	OFF	OFF	OFF
default setting				

## CPU FSB Speed Selector

Connector : SW2

Type : onboard 4-pin header

SW2	1-2	3-4
133MHz/Auto	OFF	OFF
100MHz	OFF	ON
66MHz	ON	ON
default setting		



## CMOS Operation

If the SBC refuses to boot due to inappropriate CMOS settings here is how to proceed to clear (reset) the CMOS to its default values

Connector:J6

Type:onboard 3-pin header

Mode	J6
Normal Operation	1-2
Clear CMOS	2-3
default setting	

---

## Watchdog Timer

The onboard watchdog timer can be disabled by jumper setting or enabled for either reboot by system RESET or invoking an NMI (Non-Maskable Interrupt)

Even if enabled by jumper setting upon boot the watchdog timer is always inactive. To initialize or refresh the watchdog timer writing of port 444h is sufficient. To disable the watchdog time read port 44h.

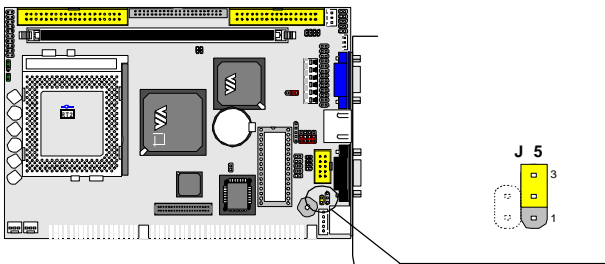
Status	Action
Enable/refresh the Watchdog Timer	I/O Write 444H
Disable the Watchdog Timer.	I/O Read 44H

After the watchdog timer has been initialized by writing port 444h, it has to be strobed at preconfigured intervals to keep it from issuing a RESET or NMI.

The watchdog timer timeout intervals are set by software programming.

### Mode Setting

Watchdog Mode	J5
Enabled for Active NMI(I/O Channel Check)	1-2
Enabled for System reset	2-3
Disable Watchdog Timer	None
default setting	



### Timeout Values

Timeout values are programmed. The watchdog timer supports 127 steps. use the table on the next page to find the hexadecimal value that needs to be passed on to get the correct timer interval. Look subsequently at the program example how to pass the value to the watchdog timer.

## Timeout Table

Level	Value	Seconds	Level	Value	Seconds	Level	Value	Seconds
1	7Fh	1	2	7Eh	2	3	7Dh	3
4	7Ch	4	5	7Bh	5	6	7Ah	6
7	79h	7	8	78h	8	9	77h	9
10	76h	10	11	75h	11	12	74h	12
13	73h	13	14	72h	14	15	71h	15
16	70h	16	17	6Fh	17	18	6Eh	18
19	6Dh	19	20	6Ch	20	21	6Bh	21
22	6Ah	22	23	69h	23	24	68h	24
25	67h	25	26	66h	26	27	65h	27
28	64h	28	29	63h	29	30	62h	30
31	61h	31	32	60h	32	33	5Fh	33
34	5Eh	34	35	5Dh	35	36	5Ch	36
37	5Bh	37	38	5Ah	38	39	59h	39
40	58h	40	41	57h	41	42	56h	42
43	55h	43	44	54h	44	45	53h	45
46	52h	46	47	51h	47	48	50h	48
49	4Fh	49	50	4Eh	50	51	4Dh	51
52	4Ch	52	53	4Bh	53	54	4Ah	54
55	49h	55	56	48h	56	57	47h	57
58	46h	58	59	45h	59	60	44h	60
61	43h	61	62	42h	62	63	41h	63
64	40h	64	65	3Fh	65	66	3Eh	66
67	3Dh	67	68	3Ch	68	69	3Bh	69
70	3Ah	70	71	39h	71	72	38h	72
73	37h	73	74	36h	74	75	35h	75
76	34h	76	77	33h	77	78	32h	78
79	31h	79	80	30h	80	81	2Fh	81
82	2Eh	82	83	2Dh	83	84	2Ch	84
85	2Bh	85	86	2Ah	86	87	29h	87
88	28h	88	89	27h	89	90	26h	90
91	25h	91	92	24h	92	93	23h	93
94	22h	94	95	21h	95	96	20h	96
97	1Fh	97	98	1Eh	98	99	1Dh	99
100	1Ch	100	101	1Bh	101	102	1Ah	102
103	19h	103	104	18h	104	105	17h	105
106	16h	106	107	15h	107	108	14h	108
109	13h	109	110	12h	110	111	11h	111
112	10h	112	113	0Fh	113	114	0Eh	114
115	0Dh	115	116	0Ch	116	117	0Bh	117
118	0Ah	118	119	09h	119	120	08h	120
121	07h	121	122	06h	122	123	05h	123
124	04h	124	125	03h	125	126	02h	126
127	01h	127						

---

## Programming Example

The following program is an examples of how to enable, disable and refresh the Watchdog timer:

```
WDT_EN_RF      equ      444h

WDT_DIS        equ      044h

WT_Enable      push  AX                ; Save AX,DX
                push  DX
                mov   DX,WDT_EN_RF    ; Enable Timer
                mov   AX,INTERVAL      ; Set Timeout Value
                out  DX,AX
                pop   DX                ; Restore DX,AX
                pop   AX
                ret

WT_Refresh     push  AX                ; Save AX,DX
                push  DX
                mov   DX,WDT_EN_RF    ; Refresh Timer
                mov   AX,INTERVAL      ; Set Timout Value
                out  DX,AX
                pop   DX                ; Restore DX,AX
                pop   AX
                ret

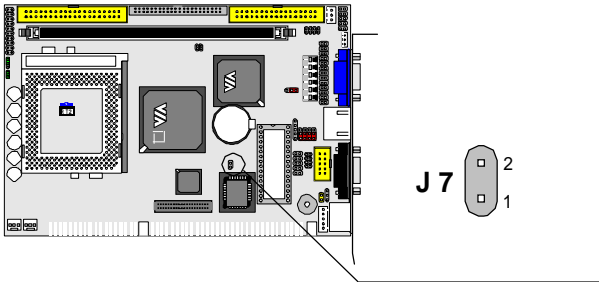
WT_Disable     push  AX                ; Save AX,DX
                push  DX
                mov   DX,WDT_DIS      ; Disable Timer
                in   AX,DX
                pop   DX                ; Restore DX,AX
                pop   AX
                ret

WT_Disable     push  AX                ; save AX,DX
                push  DX
                mov   DX,WDT_DIS      ; Disable Timer
                in   AX,DX
                pop   DX                ; restore DX,AX
                pop   AX
                ret
```

# DiskOnChip® 2000 Flash Disk

## Installation Instructions

1. Make sure the Single Board Computer is powered OFF.
2. Plug the DOC (DiskOnChip®2000) device into its socket. Verify the direction is correct (pin 1 of the DiskOnChip®2000 is aligned with pin 1 of the socket)



3. Set address

Base Address	J7
D8000h	OFF
D0000h	ON
default setting	

4. Power up the system
5. During power up you may observe a message displayed by the DOC when its drivers are automatically loaded into system's memory
6. At this stage the DOC can be accessed as any disk in the system
7. If the DOC is the only disk in the system, it will appear as the first disk (drive C: in DOS)
8. If there are more disks besides the DOC, the DOC will appear by default as the last drive, unless it was programmed as first drive. (please refer to the DOC utilities user manual)
9. If you want the DOC to be bootable:
  - a - copy the operating system files into the DOC by using the standard DOS command (for example: sys d:)
  - b - The DOC should be the only disk in the systems or should be configured as the first disk in the system (c: ) using the DUPDATE utility

For more information on DiskOnChip®2000, visit M-Systems Web site at

[http:// www.m-sys.com](http://www.m-sys.com)

where you can find the utilities manual, data sheets and application notes. In addition, you can find the latest DiskOnChip®2000 S/W utilities.

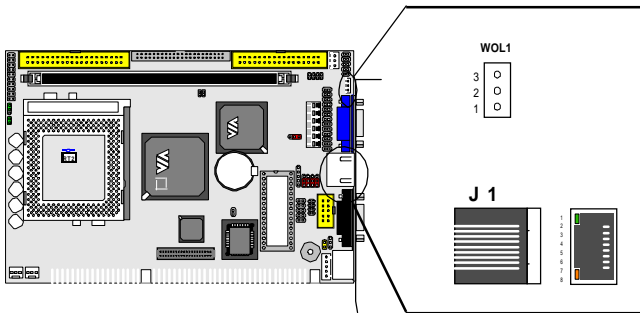
# Single Chip Fast Ethernet Controller

## LAN Port

Connector : J1

Type : external RJ-45 on bracket

Pin	1	2	3	4	5	6	7	8
Description	TX+	TX-	RX+	NC	NC	RX-	NC	NC



## LAN LED Indicator on RJ-45 connector

Connector : LED

Type : 2 LED

LED	ACT (yellow)	Speed (green)
Description	Active Transfer	100 MB mode

## Wake On LAN

Connector: WOL1

Type: onboard 3-pin wafer connector

Pin	Description
1	5V_SB
2	GND
3	WOL_CTL

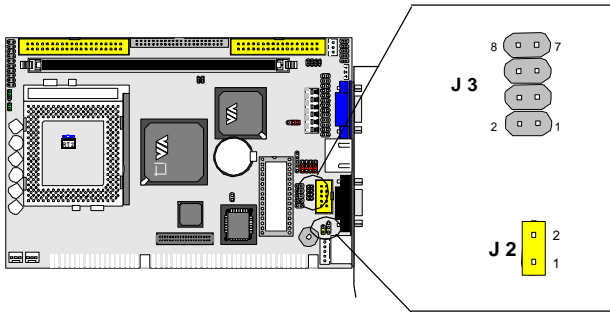


## RS-422/485 Mode on COM2

The onboard COM2 port can be configured to operate in RS-485 mode or in four different RS-422 modes. RS-422 modes differ in the way RX/TX is being handled. Jumper J2 switches between RS-232 or RS-422/485 and jumper J3 assigns the different RS-422 modes. When J2 is set all RS-232 mode settings for COM2 (JV2/JV4) are overruled.

NOTE : in RS-232 mode is COM2 assigned to onboard connector COM2  
 in RS-422/485 mode is COM2 assigned to onboard connector COM3

Mode Selection	J2
RS-232 (configure with JV2/JV4)	ON -> COM2
RS-422/485 (configure with J3)	OFF -> COM3
default setting	



Mode Selection	J3	1-2	3-4	5-6	7-8
RS-485		ON	ON	ON	ON
RS-422 TX/RX always enabled		OFF	OFF	OFF	OFF
RX enabled by RTS, TX always enabled		ON	OFF	OFF	OFF
TX enabled by RTS, RX always enabled		OFF	ON	OFF	OFF
TX/RX enabled by RTS		ON	ON	OFF	OFF
default setting					

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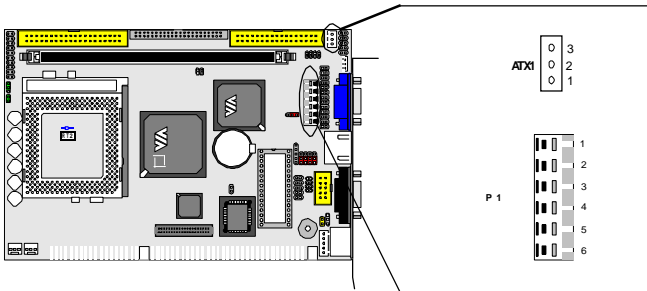
# Power Connectors

## Power Connectors

Connector : P1

Type : Onboard 6-pin AT P8 Connetor

Pin	Description
1	PWR_GOOD
2	VCC
3	+12V
4	-12V
5	GND
6	GND



Connector : ATX1

Type : Onboard 3-pin Wafer Connector

Pin	Description
1	5V SB(Standby)
2	GND
3	PS-ON

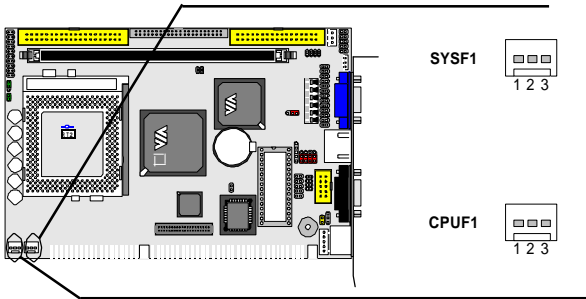
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## CPU Fan Connector

Connector : CPUF1

Type : Onboard 3-pin wafer connector

Pin	Description
1	GND
2	+12V
3	FAN_CTL



## Chassis Auxiliary Fan Connector

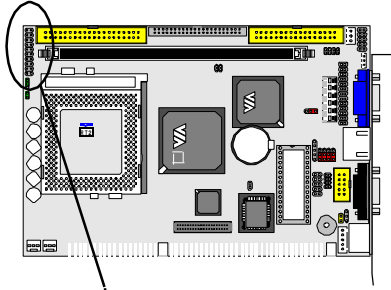
Connector : SYSF1

Type : Onboard 3-pin wafer connector

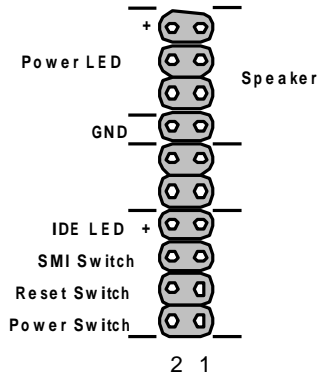
Pin	Description
1	GND
2	+12V
3	FAN_CTL

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# Switches and Indicators



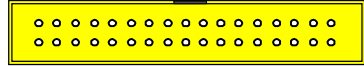
JFRT1



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## Interface Connectors HDD, FDD

### Floppy Disk Drive Connector



1

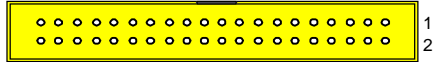
2

Connector : FDD1

Type : Onboard 34-pin box header

Pin	Description	Pin	Description
1	GND	2	DRIVE DENSITY SELECT 0
3	GND	4	DRIVE DENSITY SELECT 1
5	GND	6	NC
7	GND	8	INDEX-
9	GND	10	MOTOR ENABLE A-
11	GND	12	DRIVER SELECT B-
13	GND	14	DRIVER SELECT A-
15	GND	16	MOTOR ENABLE B-
17	GND	18	DIRECTION-
19	GND	20	STEP-
21	GND	22	WRITE DATA-
23	GND	24	WRITE GATE-
25	GND	26	TRACK 0-
27	GND	28	WRITE PROTECT-
29	GND	30	READ DATA-
31	GND	32	HEAD SELECT-
33	GND	34	DISK CHANGE-

## Enhanced IDE Connector

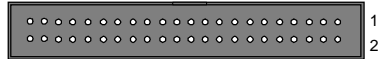


Connector : IDE1

Type : Two onboard 40-pin box headers, primary IDE

Pin	Description	Pin	Description
1	RESET	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	NC
21	REQ	22	GND
23	IOW-/STOP	24	GND
25	IOR-/HDMARDY	26	GND
27	IORDY/DDMARDY	28	IDESEL
29	DACK-	30	GND
31	IRQ	32	NC
33	A1	34	CBLID
35	A0	36	A2
37	CS0(MASTER CS)	38	CS1(SLAVE CS)
39	LED ACT-	40	GND

## Enhanced IDE Connector



IDE2

Connector : IDE2

Type : Onboard 44-pin box headers, secondary IDE

Pin	Description	Pin	Description
1	RESET	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	N C
21	REQ	22	GND
23	IOW-/STOP	24	GND
25	IOR-/HDMARDY	26	GND
27	IRDY/DDMARDY	28	IDESEL
29	DACK-	30	GND
31	IRQ	32	N C
33	A1	34	CBLID
35	A0	36	A2
37	CS0(MASTER CS)	38	CS1(SLAVE CS)
39	LED ACT-	40	GND
41	VCC	42	VCC
43	GND	44	GND

# Peripheral Ports

## Parallel Port

Connector : LPT1

Type : Onboard 26-pin header



**LPT1**

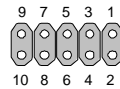
Pin	Description	Pin	Description
1	STROBE-	14	AUTO FEED-
2	DATA0	15	ERROR-
3	DATA1	16	INITIALIZE-
4	DATA2	17	SELECT INPUT-
5	DATA3	18	GND
6	DATA4	19	GND
7	DATA5	20	GND
8	DATA6	21	GND
9	DATA7	22	GND
10	ACKNOWLEDGE-	23	GND
11	BUSY	24	GND
12	PAPER EMPTY	25	GND
13	SELECT+	26	NC

## USB Ports

Connector: USB1

Type: onboard 10-pin header for two USB ports

**USB1**

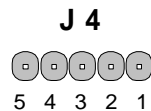


Pin	Description	Pin	Description
1	VCC	2	VCC
3	DATA0-	4	DATA1-
5	DATA0+	6	DATA1+
7	GND	8	GND
9	GND	10	GND

## IrDA

Connector : J4

Type : onboard 5-pin header

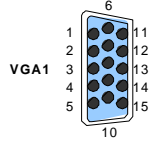


Pin	Description	Pin	Description
1	Vcc	2	NC
3	IRRX	4	GND
5	IRTX		

## CRT SVGA

Connector : VGA1

Type : external 15-pin D-sub female connector on bracket

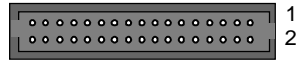


Pin	Description	Pin	Description	Pin	Description
1	RED	6	GND	11	NC
2	GREEN	7	GND	12	VDDAT
3	BLUE	8	GND	13	HSYNC
4	NC	9	Vcc	14	VSYNC
5	GND	10	GND	15	VDCLK

## TMDS LCD / External TV Encoder Port

Connector:JLCD1

Type:42-pin onboard header

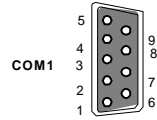


Pin	Description	Pin	Description
1	PCIRST-	2	GND
3	USB_DT3+	4	USB_DT3-
5	GND	6	OC0(USB Over-Current)
7	VCC	8	GND
9	GND	10	VCC3
11	VCC	12	GND
13	GND	14	VCC3
15	FP_D11/TV_BLANK	16	GND
17	FP_DET/TV_D11	18	SPD1(Serial Port Data)
19	FP_D10/TV_D10	20	GND
21	FP_D9/TV_D9	22	SPCLK1(Serial Port Clock)
23	FP_D8/TV_D8	24	GND
25	FP_D7/TV_D7	26	GOPO
27	FP_D6/TV_D6	28	GND
29	FP_D5/TV_D5	30	FP_DEN/TV_CLK
31	FP_D4/TV_D4	32	GND
33	FP_D3/TV_D3	34	FP_CLK/TV_CLKR
35	FP_D2/TV_D2	36	GND
37	FP_D1/TV_D1	38	FP_VS/TV_VS(VSYNC)
39	FP_D0/TV_D0	40	GND
41	GND	42	FP_HS/TV_HS(HSYNC)

## COM1 RS-232C Ports on bracket

Connector : COM1

Type : external 9-pin D-sub male connector on bracket

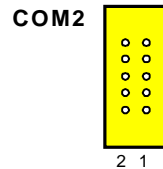


Pin	Description	Pin	Description
1	DCD (or POS mode +5V)	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI (or POS mode +12V)		

## COM2 onboard RS-232C Port

Connector : COM2

Type : onboard 10-pin box header

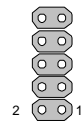


Pin	Description	Pin	Description
1	DCD (or POS mode +5V)	2	RXD
3	TXD	4	DTR
5	GND	6	DSR
7	RTS	8	CTS
9	RI (or POS mode +12V)	10	NC

## COM3 onboard RS-422/485 Port

Connector : COM3

Type : onboard 10-pin header



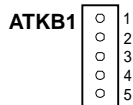
Pin	Description	Pin	Description
1	TX-	2	TX+
3	RX+	4	RX-
5	GND	6	RTS-
7	RTS+	8	CTS+
9	CTS-	10	NC

---

## AT Keyboard

Connector : ATKB1

Type : Onboard 5-pin header



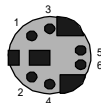
Pin	Description	Pin	Description
1	CLK	2	DATA
3	N/C	4	GND
5	N/C		

Note: ATKB1 doesn't provide Vcc power pin on pin-5, that is, ATKB1 cannot connect to AT keyboard directly. ATKB1 supports AT keyboard with passive backplane.

## PS/2 Keyboard & Mouse

Connector: KB1

Type: external 6-pin Mini DIN connector on bracket



Pin	Description	Pin	Description
1	KB-DATA	2	MS-DATA
3	GND	4	VCC
5	KB-CLK	6	MS-CLK

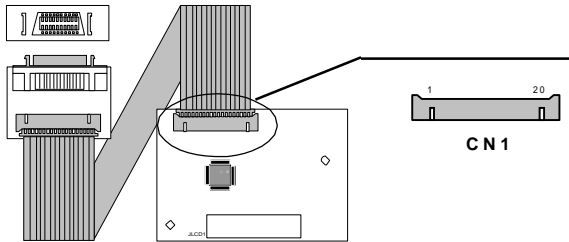
Note: KB1 supports PS/2 keyboard directly, and PS/2 mouse supported with the additional PS2 1-to-2 cable in the standard packing.

---

## Interface Daughter Board

### TMDS Panel Link Daughter Board (Optional) (3901140)

This daughter board connects to JLCD1 of SBC.



Connector : CN1

Type : Onboard 20-pin header

Pin	Description	Pin	Description
1	VCC	11	FP AGND
2	FP AGND	12	TXC+
3	TX2+	13	TXC-
4	TX2-	14	FP AGND
5	FP AGND	15	USBDT+
6	TX1+	16	USBDT-
7	TX1-	17	FP AGND
8	FP AGND	18	SPCLK1
9	TX0+	19	SPD1
10	TX0-	20	FPDET

---

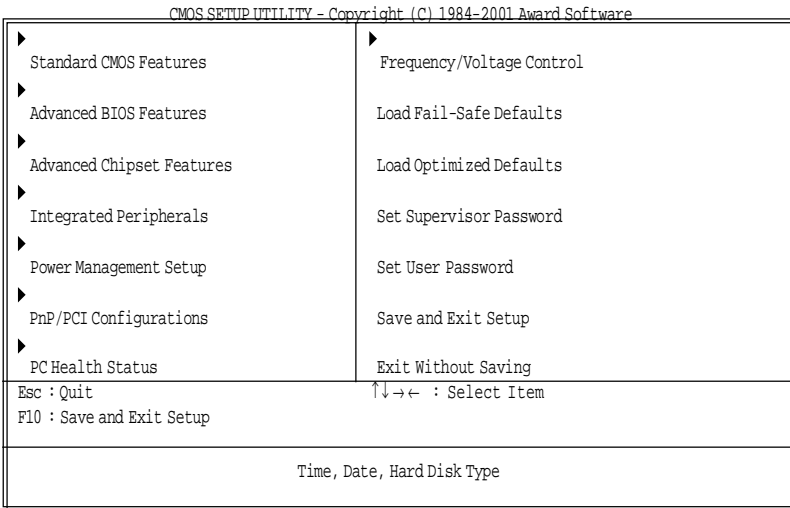
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## AWARD BIOS Setup

The SBC uses the Award PCI/ISA BIOS ver 6.0 for the system configuration. The Award BIOS setup program is designed to provide the maximum flexibility in configuring the system by offering various options which could be selected for end-user requirements. This chapter is written to assist you in the proper usage of these features.

To access AWARD PCI/ISA BIOS Setup program, press <Del> key. The Main Menu will be displayed at this time.



Once you enter the AwardBIOS™ CMOS Setup Utility, the Main Menu will appear on the screen. The Main Menu allows you to select from several setup functions and two exit choices. Use the arrow keys to select among the items and press <Enter> to accept and enter the sub-menu.

---

## Setup Items

The main menu includes the following main setup categories. Recall that some systems may not include all entries.

### Standard CMOS Features

Use this menu for basic system configuration.

### Advanced BIOS Features

Use this menu to set the Advanced Features available on your system.

### Advanced Chipset Features

Use this menu to change the values in the chipset registers and optimize your system's performance.

### Integrated Peripherals

Use this menu to specify your settings for integrated peripherals.

### Power Management Setup

Use this menu to specify your settings for power management.

### PnP / PCI Configuration

This entry appears if your system supports PnP / PCI.

### Frequency/Voltage Control

Use this menu to specify your settings for frequency/voltage control.

### Load Fail-Safe Defaults

Use this menu to load the BIOS default values for the minimal/stable performance for your system to operate.

### Load Optimized Defaults

Use this menu to load the BIOS default values that are factory settings for optimal performance system operations. While Award has designed the custom BIOS to maximize performance, the factory has the right to change these defaults to meet their needs.

### Supervisor / User Password

Use this menu to set User and Supervisor Passwords.

### Save & Exit Setup

Save CMOS value changes to CMOS and exit setup.

### Exit Without Save

Abandon all CMOS value changes and exit setup.

## Standard CMOS Setup

CMOS SETUP UTILITY - Copyright (C) 1984-2001 Award Software		Item Help
Standard CMOS Features		
Date:	Fri, Feb 23 2001	Change the day, month, year and century
Time:	16:19:20	
▶ IDE Primary Master	[None]	
▶ IDE Primary Slave	[None]	
▶ IDE Secondary Master	[None]	
▶ IDE Secondary Slave	[None]	
Drive A	1.44M, 3.5 in.	
Drive B	[None]	
Video	[EGA/VGA]	
Halt On	[All , but Keyboard]	
Base Memory	640K Extended	
Memory	252928K	
Total Memory	253952K	

↑ ↓ ← → Move Enter: Select +/- /PU/PD: Value F10: Save ESC: Exit F1: General Help  
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

### Date

The BIOS determines the day of the week from the other date information; this field is for information only.

### Time

The time format is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Press the « or ( key to move to the desired field . Press the PgUp or PgDn key to increment the setting, or type the desired value into the field.

### IDE Primary Master/Slave

### IDE Secondary Master/Slave

Options are in sub menu (see page 30)

### Drive A, B

Select the correct specifications for the diskette drive(s) installed in the computer.

None :	No diskette drive installed
360K ;	5.25 in 5-1/4 inch PC-type standard drive
1.2M ;	5.25 in 5-1/4 inch AT-type high-density drive
720K ;	3.5 in 3-1/2 inch double-sided drive
1.44M ;	3.5 in 3-1/2 inch double-sided drive
2.88M ;	3.5 in 3-1/2 inch double-sided drive

---

**Video** Select the type of primary video subsystem in your computer. The BIOS usually detects the correct video type automatically. The BIOS supports a secondary video subsystem, but you do not select it in Setup.

**Halt On** During the power-on self-test (POST), the computer stops if the BIOS detects a hardware error. You can tell the BIOS to ignore certain errors during POST and continue the boot-up process. These are the selections:

No errors	POST does not stop for any errors.
All errors	If the BIOS detects any non-fatal error, POST stops and prompts you to take corrective action.
All, But Keyboard	POST does not stop for a keyboard error, but stops for all other errors.
All, But Diskette	POST does not stop for diskette drive errors, but stops for all other errors.
All, But Disk/Key	POST does not stop for a keyboard or disk error, but stops for all other errors.

## IDE Harddisk Setup (submenu)

CMOS SETUP UTILITY - Copyright (C) 1984-2001 Award Software	
IDE Primary Master	
IDE HDD Auto-Detection	Item Help
IDE HDD Auto-Detection	Press Enter
IDE Primary Master	[Auto] Menu Level ▶▶
Access Mode	[Auto]
Capacity	0 MB
Cylinder	0
Head	0
Precomp	0
Landing Zone	0
Sector	0

↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help  
F5:Previous Values F6:Fail-Safe Defaults F7:Optimized Defaults

### IDE HDD Auto-detection

Press Enter to auto-detect the HDD on this channel. If detection is successful, it fills the remaining fields on this menu.

### IDE Primary Master

Selecting 'manual' lets you set the remaining fields on this screen. Selects the type of fixed disk. "User Type" will let you select the number of cylinders, heads, etc. Note: PRECOMP=65535 means NONE !

### Capacity

Disk drive capacity (Approximated). Note that this size is usually slightly greater than the size of a formatted disk given by a disk checking program.

### Access Mode

Normal, LBA, Large or Auto Choose the access mode for this hard disk

---

The following options are selectable only if the 'IDE Primary Master' item is set to 'Manual'

Cylinder            Min = 0   Max = 65535  
Set the number of cylinders for this hard disk.

Head                Min = 0   Max = 255  
Set the number of read/write heads

Precomp            Min = 0   Max = 65535  
\*\*\*\* Warning: Setting a value of 65535 means no hard disk

Landing zone      Min = 0   Max = 65535  
\*\*\*\* Warning: Setting a value of 65535 means no hard disk

Sector             Min = 0   Max = 255  
Number of sectors per track

We recommend that you select Type "AUTO" for all drives. The BIOS will auto-detect the hard disk drive and CD-ROM drive at the POST stage.

If your hard disk drive is a SCSI device, please select "None" for your hard drive setting.

## BIOS Features Setup

CMOS SETUP UTILITY - Copyright (C) 1984-2001 Award Software		
Advanced BIOS Features		
		Item Help
Virus Warning	[Enabled]	Menu Level ▶  Allows you to choose the VIRUS warning feature for IDE Hard Disk boot sector protection. If this function is enabled and someone attempt to write data into this area, BIOS will show a warning message on screen and alarm beep
CPU Internal Cache	[Enabled]	
External Cache	[Enabled]	
CPU L2 Cache ECC Checking	[Enabled]	
Processor Number Feature	[Enabled]	
Quick Power On Self Test	[Disabled]	
First Boot device	[Floppy]	
Second Boot device	[HDD-0] Third	
Boot device	[Floppy] Boot	
other device	[Disabled]	
Swap Floppy Drive	[Disabled]	
Boot Up Floppy Seek	[Disabled]	
Boot Up NumLock Status	[Off] Gate	
A20 Option	[Normal]	
Typematic Rate Setting	[Disabled]	
Typematic Rate (Chars/Sec)	6	
Typematic Delay (Msec)	250	
Security Option	[Setup] OS	
Select For DRAM > 64MB	[Non-OS2]	
Video BIOS Shadow	[Enabled]	
C8000-CBFFF Shadow	[Disabled]	
CC000-CFFFF Shadow	[Disabled]	
D0000-D3FFF Shadow	[Disabled]	
D4000-D7FFF Shadow	[Disabled]	
D8000-DBFFF Shadow	[Disabled]	
DC000-DFFFF Shadow	[Disabled]	

↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help  
 F5:Previous Values F6:Fail-Safe Defaults F7:Optimized Defaults

### Virus Warning

Allows you to choose the VIRUS Warning feature for IDE Hard Disk boot sector protection. If this function is enabled and someone attempt to write data into this area, BIOS will show a warning message on screen and beep.

**Enabled** Activates automatically when the system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table.

**Disabled** No warning message will appear when anything attempts to access the boot sector or hard disk partition table.

---

### CPU Internal Cache/External Cache

These two categories speed up memory access. However, it depends on CPU/chipset design. Enabled : Enable cache, Disabled : Disable cache

### CPU L2 Cache ECC Checking

This item allows you to enable/disable CPU L2 Cache ECC checking.  
The choice: Enabled, Disabled.

### Processor Number Feature

This feature appears when a Pentium III processor is installed. It enables you enables you to control whether the Pentium III's serial number can be read by external programs. The choice : Enabled. Disabled

### Quick Power On Self Test

This category speeds up Power On Self Test (POST) after you power up the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST. Enabled : Enable quick POST. Disabled : Normal POST

### First/Second/Third/Other Boot Device

The BIOS attempts to load the operating system from the devices in the sequence selected in these items. The choices are : Floppy, LS/ZIP, HDD, SCSI, CDROM, Disabled.

### Swap Floppy Drive

If the system has two floppy drives, you can swap the logical drive name assignments. The choice: Enabled/Disabled.

### Boot Up Floppy Seek

Seeks disk drives during boot up. Disabling speeds boot up.  
The choice: Enabled/Disabled.

### Boot Up NumLock Status

Select power on state for NumLock. The choice: Enabled/Disabled.

### Gate A20 Option

Select if chipset or keyboard controller should control GateA20.

Normal A pin in the keyboard controller controls GateA20

Fast Lets chipset control GateA20

### Typematic Rate Setting

Key strokes repeat at a rate determined by the keyboard controller. When enabled, the typematic rate and typematic delay can be selected.

The choice: Enabled/Disabled.

### Typematic Rate (Chars/Sec)

Sets the number of times a second to repeat a key stroke when you hold the key down. The choice: 6, 8, 10, 12, 15, 20, 24, 30.

### Typematic Delay (Msec)

Sets the delay time after the key is held down before it begins to repeat the keystroke. The choice: 250, 500, 750, 1000.

---

### Security Option

Select whether the password is required every time the system boots or only when you enter setup.

**System** The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.

**Setup** The system will boot, but access to Setup will be denied if the correct password is not entered at the prompt.

**Note** To disable security, select PASSWORD SETTING at Main Menu and then you will be asked to enter password. Do not type anything and just press <Enter>, it will disable security. Once the security is disabled, the system will boot and you can enter Setup freely.

### OS Select For DRAM > 64MB

Select the operating system that is running with greater than 64MB of RAM on the system. The choice: Non-OS2, OS2.

### Video BIOS Shadow

Enabled this copies the video BIOS from ROM to RAM. effectively enhancing performance, and reducing the amount of upper memory available by 32KB (the C0000-C7FFF area of memory between 640 KB and 1 MB is used).

### C8000-CBFFF Shadow

Enabling any of the C8000-CBFFF segments allows components to move their firmware into these upper memory segments. However your computer can lock-up doing so, because some devices don't like being shadowed at those particular 16 KB segments of upper memory.

**Note** - In Windows 95, double click 'Computer' within Device Manager and select 'Memory'. This will tell you what segments (if any) are being shadowed  
For DOS you can use MSD.EXE to see what segments are claimed.

CC000-CFFFF - D0000-D3FFF - D4000-D7FFF - D8000-DBFFF and  
DC000-DFFFF - Same as above.

## Chipset Features Setup

CMOS SETUP UTILITY - Copyright (C) 1984-2001 Award Software Advanced Chipset Features		
		Item Help
DRAM Timing by SPD		
DRAM Clock	Host CLK	
SDRAM Cycle Length	3	Menu Level ▶
Bank Interleave	Disabled	
Memory Hole	[Disabled]	Allows you to choose the VIRUS warning feature for IDE Hard
P2C/C2P Concurrency	[Enabled]	Diskboot sector protection. If this function is enabled and someone attempt to write data
Fast R-W Turn Around	[Disabled]	into this area, BIOS will show a warning message on screen and
System BIOS Cacheable	[Disabled]	alarm beep
Frame Buffer Size	[8M] AGP	
Aperture Size	[64M]	
AGP-4X Mode	[Enabled]	
AGP Driving Control	[Auto] AGP	
Driving Value	DA OnChip	
USB	[Enabled]	
USB Keyboard Support	[Disabled]	
OnChip Sound	[Auto] CPU to	
PCI Write Buffer	[Enabled]	
PCI Dynamic Bursting	[Enabled]	
PCI Delay Transaction	[Disabled]	
PCI#2 Access #1 Retry	[Enabled]	
AGP Master 1 WS Write	[Enabled]	
AGP Master 1 WS Read	[Disabled]	

↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help  
F5:Previous Values F6:Fail-Safe Defaults F7:Optimized Defaults

### DRAM Timing By SPD

If your DIMM memory have SPD ( Serial Presence Detect ) 8-pin IC on module, you can set this option to Enabled. System will set your DRAM clock and timing from the SPD IC. If the option set as Disabled, DRAM clock and timing must be set from items below. (DRAM Clock, SDRAM Cycle Length and Bank Interleave)

### DRAM Clock

This item allows you to set the DRAM Clock. Options are Host CLK, HCLK+33M or HCLK-33M. Please set the item according to the Host (CPU) Clock and DRAM Clock.

### SDRAM Cycle Length

This feature is similar to SDRAM CAS Latency Time. It controls the time delay (in clock cycles - CLKs) that passes before the SDRAM starts to carry out a read command after receiving it. This also determines the number of CLKs for the completion of the first part of a burst transfer. Thus, the lower the cycle length, the faster the transaction. However, some SDRAM cannot handle the lower cycle length and may become unstable. So, set the SDRAM Cycle Length to 2 for optimal performance if possible but increase it to 3 if your system becomes unstable.

---

### Bank Interleave

This feature enables you to set the interleave mode of the SDRAM interface. Interleaving allows banks of SDRAM to alternate their refresh and access cycles. One bank will undergo its refresh cycle while another is being accessed. This improves performance of the SDRAM by masking the refresh time of each bank. A closer examination of interleaving will reveal that since the refresh cycles of all the SDRAM banks are staggered, this produces a kind of pipelining effect. If there are 4 banks in the system, the CPU can ideally send one data request to each of the SDRAM banks in consecutive clock cycles. This means in the first clock cycle, the CPU will send an address to Bank 0 and then send the next address to Bank 1 in the second clock cycle before sending the third and fourth addresses to Banks 2 and 3 in the third and fourth clock cycles respectively. Each SDRAM DIMM consists of either 2 banks or 4 banks. 2-bank SDRAM DIMMs use 16Mbit SDRAM chips and are usually 32MB or less in size. 4-bank SDRAM DIMMs, on the other hand, usually use 64Mbit SDRAM chips though the SDRAM density may be up to 256Mbit per chip. All SDRAM DIMMs of at least 64MB in size or greater are 4-banked in nature.

If you are using a single 2-bank SDRAM DIMM, set this feature to 2-Bank. But if you are using two 2-bank SDRAM DIMMs, you can use the 4-Bank option as well. With 4-bank SDRAM DIMMs, you can use either interleave options. Naturally, 4-bank interleave is better than 2-bank interleave so if possible, set it to 4-Bank. Use 2-Bank only if you are using a single 2-bank SDRAM DIMM. Notethat it is recommends that SDRAM bank interleaving be disabled if 16Mbit SDRAM DIMMs are used.

### Memory Hole

Enabling this feature reserves 15MB to 16MB memory address space to ISA expansion cards that specifically require this setting. This makes the memory from 15MB and up unavailable to the system. Expansion cards can only access memory up to 16MB.

### P2C/C2P Concurrency

When Disabled, CPU bus will be occupied during the entire PCI operation period.

### Fast R-W Turn Around

This BIOS option reduces the delay that occurs when the CPU first reads from the RAM and then writes to it. There is normally an extra delay associated with this switch from reading to writing. If you enable this option, the delay will be reduced and switching from read to write will be faster. However, if your RAM modules cannot handle the faster turnaround, data may be lost and your system may become unstable. With that in mind, enable this option for better RAM performance unless you face stability problems after enabling it.

### System BIOS Cacheable

Allows the system BIOS to be cached for faster system performance.

### Frame Buffer Size

This item defines the amount of system memory that will be shared and uses as video memory.

---

## AGP Aperture Size

Options : 4, 8, 16, 32, 64, 128, 256

This option selects the size of the AGP aperture. The aperture is a portion of the PCI memory address range dedicated as graphics memory address space. Host cycles that hit the aperture range are forwarded to the AGP without need for translation. This size also determines the maximum amount of system RAM that can be allocated to the graphics card for texture storage.

AGP Aperture size is set by the formula : maximum usable AGP memory size x 2 plus 12MB. That means that usable AGP memory size is less than half of the AGP aperture size. That's because the system needs AGP memory (un-cached) plus an equal amount of write combined memory area and an additional 12MB for virtual addressing. This is address space, not physical memory used. The physical memory is allocated and released as needed only when Direct3D makes a "create non-local surface" call.

## AGP-4X Mode

Set to Enabled if your AGP card supports the 4X mode, which transfers video data at 1066MB/s.

## AGP Driving Control

This item is use for control AGP drive strength.

Auto: Setup AGP drive strength by default setting.

Manual: Setup AGP drive strength by manual setting.

## AGP Driving Value

Key in a HEX number to control AGP output buffer drive strength.

Min = 00, Max = FF.

## OnChip USB

If your system contains a Universal Serial Bus controller and you have a USB peripheral, select Enabled. The next option will become available.

## USB Keyboard Support

This item lets you enable or disable the USB keyboard driver within the onboard BIOS.

## CPU to PCI Write Buffer

This controls the CPU write buffer to the PCI bus. If this buffer is disabled, the CPU writes directly to the PCI bus. Although this may seem like the faster and thus, the better method, this isn't true. Because the CPU bus is faster than the PCI bus, any CPU writes to the PCI bus has to wait until the PCI bus is ready to receive data. This prevents the CPU from doing anything else until it has completed sending the data to the PCI bus. Enabling the buffer enables the CPU to immediately write up to 4 words of data to the buffer so that it can continue on another task without waiting for those 4 words of data to reach the PCI bus. The data in the write buffer will be written to the PCI bus when the next PCI bus read cycle starts. The difference here is that it does so without stalling the CPU for the entire CPU to PCI transaction. Therefore, it's recommended that you enable the CPU to PCI write buffer.

---

### PCI Dynamic Bursting

When enabled, data transfer on the PCI bus, where possible, make use of the high-performance PCI burst protocol, in which greater amounts of data are transferred at a single command.

### PCI Master 0 WS Write

This function determines whether there's a delay before any writes to the PCI bus. If this is enabled, then writes to the PCI bus are executed immediately (with zero wait states), as soon as the PCI bus is ready to receive data. But if it is disabled, then every write transaction to the PCI bus is delayed by one wait state. Normally, it's recommended that you enable this for faster PCI performance. However, disabling it may be useful when overclocking the PCI bus results in instability. The delay will generally improve the overclockability of the PCI bus.

### PCI Delay Transaction

The chipset has an embedded 32-bit posted write buffer to support delay transactions cycles. Select Enabled to support compliance with PCI specification version 2.1.

### PCI # 2 Access # 1 Retry

This BIOS feature is linked to the CPU to PCI Write Buffer. Normally, the CPU to PCI Write Buffer is enabled. All writes to the PCI bus are, as such, immediately written into the buffer, instead of the PCI bus. This frees up the CPU from waiting till the PCI bus is free. The data are then written to the PCI bus when the next PCI bus cycle starts.

There's a possibility that the buffer write to the PCI bus may fail. When that happens, this BIOS option determines if the buffer write should be reattempted or sent back for arbitration. If this BIOS option is enabled, then the buffer will attempt to write to the PCI bus until successful. If disabled, the buffer will flush its contents and register the transaction as failed. The CPU will have to write again to the write buffer. It is recommended that you enable this feature unless you have many slow PCI devices in your system. In that case, disabling this feature will prevent the generation of too many retries which may severely tax the PCI bus.

### AGP Master 1 WS Write

By default, the AGP busmastering device waits for at least 2 wait states or AGP clock cycles before it starts a write transaction. This BIOS option allows you to reduce the delay to only 1 wait state or clock cycle. For better AGP write performance, enable this option but disable it if you experience weird graphical anomalies like wireframe effects and pixel artifacts after enabling this option.

### AGP Master 1 WS Read

By default, the AGP busmastering device waits for at least 2 wait states or AGP clock cycles before it starts a read transaction. This BIOS option allows you to reduce the delay to only 1 wait state or clock cycle. For better AGP read performance, enable this option but disable it if you experience weird graphical anomalies like wireframe effects and pixel artifacts after enabling this option.

## Integrated Peripherals

CMOS SETUP UTILITY - Copyright (C) 1984-2001 Award Software Integrated Peripherals		
OnChip IDE Channel0	[Enabled]	ItemHelp
OnChip IDE Channel1	[Enabled]	
IDE Prefetch Mode	[Enabled]	Menu Level ▶
Primary Master PIO	[Auto]	Allows you to choose the VIRUS warning feature for IDE Hard
Primary Slave PIO	[Auto]	Diskboot sector protection. If
Secondary Master PIO	[Auto]	this function is enabled and
Secondary Slave PIO	[Auto]	someone attempt to write data
Primary Master UDMA	[Auto]	into this area, BIOS will show
Primary Slave UDMA	[Auto]	a warning message on screen and
Secondary Master UDMA	[Auto]	alarm beep
Secondary Slave UDMA	[Auto] Init	
Display First	[PCI Slot]	
IDE HDD Block Mode	[Enabled]	
Onboard FDD Controller	[Enabled]	
Onboard Serial Port 1	[Auto]	
Onboard Serial Port 2	[Auto] UART 2	
Mode	[Standard]	
IR Function Duplex	Half Tx, Rx	
invertig enable	No, Yes	
Onboard Parallel Port	[378/IRQ7]	
Onboard Parallel Mode	[Normal] ECP	
Mode Use DMA	3	
Parallel Port EPP Type	EPP1.9	
Onboard Legacy Audio	[Enabled]	
Sound Blaster	[Disabled]	
SB I/O Base Address	[220H] SB IRQ	
Select	[IRQ 5] SB	
DMA Select	[DMA1]	
MPU-401	[Disabled]	
MPU-401 I/O Address	[330-333H]	

↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help  
F5:Previous Values F6:Fail-Safe Defaults F7:Optimized Defaults

### OnChip IDE Channel 0/1

Select "Enabled" to activate each on-board IDE channel separately, Select "Disabled", if you install an add-on IDE Control card

### IDE Prefetch Mode

Enable prefetching for IDE drive interfaces that support its faster drive accesses. If you are getting disk drive errors, change the setting to omit the drive interface where the errors occur. Depending on the configuration of your IDE subsystem, this field may not appear, and it does appear when the Internal PCI/IDE filed, above, is Disabled.

---

### Primary & Secondary Master/Slave PIO

These four PIO fields let you set a PIO mode (0-4) for each of four IDE devices. When under "Auto" mode, the system automatically set the best mode for each device

### Primary & Secondary Master/Slave UDMA

When set to "Auto" mode, the system will detect if the hard drive supports Ultra DMA mode.

### Init Display First

Select "AGP" or "PCI Slot" for system to detect first when boot-up.

### IDE HDD Block Mode

This feature enhances disk performance by allowing multi-sector data transfers and eliminates the interrupt handling time for each sector.

### Onboard FDD Controller

Select "Enabled" to activate the on-board FDD

Select "Disabled" to activate an add-on FDD

### Onboard Serial Port 1 & 2

Select an address and corresponding interrupt for the first/second serial port. The default value for the first serial port is "3F8/IRQ4" and the second serial port is "2F8/IRQ3".

### UART 2 Mode

Select to activate the Infrared transfer function.

### Onboard Parallel Port

Select address and interrupt for the Parallel port.

### Onboard Parallel Mode

Select an operating mode for the parallel port. Mode options are Normal, EPP, ECP, ECP/EPP.

### ECP Mode Use DMA

Select a DMA channel if parallel Mode is set as ECP, ECP/EPP.

### Parallel Port EPP Type

Select a EPP Type if parallel Port is set as EPP, ECP/EPP.

### Onboard Legacy Audio

Configuration options: Enabled and Disabled. When Enabled, select additional settings for SoundBlaster Compatibility and MPU-401 functionality

## Power Management Setup

CMOS SETUP UTILITY - Copyright (C) 1984-2001 Award Software	
Power Management Setup	
ACPI function	<b>Disabled</b>
▶ Power Management	[Press Enter]
ACPI Suspend Type	[S1 (POS)] PM
Control by APM	[Yes] Video Off
Option	[Suspend -> Off]
Video Off Method	[V/H SYNC+Blank]
MODEM Use IRQ	[3]
Soft-off by PWRBTN	[Instant-Off]
▶ Wake Up Events	[Press Enter]

Item Help

Menu Level ▶

↑↓ → ← : Move Enter: Select +/- /PU/PD: Value F10: Save ESC: Exit F1: General Help  
 F5: Previous Values F6: Fail-Safe Defaults F7: Optimized Defaults

### ACPI Function

Select Enabled only if your computer's operating system supports ACPI (the Advanced Configuration and Power Interface) specification. Currently, Windows 98 and Windows2000 support ACPI.

### Power Management

There are 4 selections for Power Management, 3 of which have fixed mode :

- |                    |  |
|--------------------|--|
| Disabled (default) | No power management. Disables all four modes.  |
| Min. Power Saving  | Minimum power management. Doze Mode = 1 hr., Standby Mode = 1 hr., Suspend Mode = 1 hr.,                                   |
| Max. Power Saving  | Maximum power management -- ONLY AVAILABLE FOR SL CPU's.. Doze Mode = 1 min., Standby Mode = 1 min., Suspend Mode = 1 min. |
| User Defined       | Allows you to set each mode individually. When not disabled, each of the ranges are from 1 min. to 1 hr.                   |

HDD Power Down is always set independently

---

## ACPI Suspend Type

### S1 (POS) Power On suspend

All devices are powered up except for the clock synthesizer. The Host and PCI clocks are inactive and PIIX4 provides control signals and 32-kHz Suspend Clock (SUSCLK) to allow for DRAM refresh and to turn off the clock synthesizer. The only power consumed in the system is due to DRAM Refresh and leakage current of the powered devices. When the system resumes from POS, PIIX4 can optionally resume without resetting the system, can reset the processor only, or can reset the entire system. When no reset is performed, PIIX4 only needs to wait for the clock synthesizer and processor PLLs to lock before the system is resumed. This takes typically 20 ms.

### S3 (STR) Suspend To RAM

Power is removed from most of the system components during STR, except the DRAM. Power is supplied to Suspend Refresh logic in the Host Controller, and RTC and Suspend Well logic in PIIX4. PIIX4 provides control signals and 32-kHz Suspend Clock (SUSCLK) to allow for DRAM refresh and to turn off the clock synthesizer and other power planes.

### PM Control By APM

When enabled, an Advanced power Management device will be activated to enhance the Max. Power Saving mode and stop the CPU internal clock. If the Max. Power Saving is not enabled, this will be preset to No.

### Video Off Option

Controls what causes the display to be switched off

Suspend -> Off                      Always On                      All Mode -> Off

### Video Off Method

This determines the manner in which the monitor is blanked.

V/H SYNC+Blank                      cause the system to turn off the vertical and horizontal synchronization signals and writes blanks to the screen.

Blank Screen                          This option only writes blanks to the screen.

DPMS                                      Initial display power management signaling.

### Modem Use IRQ

Name the interrupt request (IRQ) assigned to the modem (if any) on your system. Activity of the selected IRQ always awakens the system.

### Soft-Off By PWRBTN

The field defines the power-off mode when using an ATX power supply. The Instant-Off mode means powering off immediately when pressing the power button. In the Delay 4 Sec mode, the system powers off when the power button is pressed for more than four seconds or places the system in a very low-power-usage state, with only enough circuitry receiving power to detect power button activity or resume by ring activity when press for less than four seconds. The default is 'Instant-Off'.

---

## Wake Up Events

Setting an event on each device listed to awaken the system from a soft off state.

VGA

LPT & COM

HDD & FDD

PCI Master

Power On by PCI Card

Wake Up on LAN/Ring

RTC Alarm Resume

Date (of Month)

Resume Time (hh:mm:ss)

Primary INTR

IRQs Activity Monitoring

## PnP/PCI Configuration

CMOS SETUP UTILITY - Copyright (C) 1984-2001 Award Software		
Power Management Setup		
		Item Help
PnP OS Installed	[No]	
Reset Configuration Data	[Disabled]	Menu Level ▶
Resource Controlled By	[Auto(ESCD)]	
▶ IRQ Resources	Press Enter	Select Yes if you are
▶ DMA Resources	Press Enter	using a Plug and Play PCI/VGA
Palette Snoop	[Disabled]	capable operating
Assign IRQ For VGA	[Disabled]	system Seelct No if
Assign IRQ For USB	[Enabled]	need the BIOS to
		configure non-boot
		devices

↑↓→←:Move Enter:Select +/-/PU/PD:Value F10:Save ESC:Exit F1:General Help

F5:Previous Values F6:Fail-Safe Defaults F7:Optimized Defaults

This section describes configuring the PCI bus system. PCI, or Personal Computer Interconnect, is a system which allows I/O devices to operate at speeds nearing the speed the CPU itself uses when communicating with its own special components.

### PnP OS Installed

Select Yes if the system operating environment is Plug-and-Play aware (e.g., Windows 95).

### Reset Configuration Data

Normally, you leave this field Disabled. Select Enabled to reset ESCD (Extended System Configuration Date) when you exit Setup if you have installed a new add-on and the system reconfiguration has caused such a serious conflict that the operating system cannot boot.

### Resource Controlled By

The Award Play and Play BIOS can automatically configure all the boot and Plug-and-Play compatible devices. If you select Auto, all the interrupt request (IRQ) and DMA assignment fields disappear, as the BIOS automatically assigns them.

---

### IRQ Resources

When resources are controlled manually, assign each system interrupt as one of the following types, depending on the type of device using the interrupt :

- Legacy ISA     Devices compliant with the original PC/AT bus specification, requiring a specific interrupt (such as IRQ4 for serial port 1).
- PCI/ISA PnP    Device compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

### DMA Resources

When resources are controlled manually, assign each system DMA channel as one of the following types, depending on the type of device using the DMA :

- Legacy ISA     Devices compliant with the original PC/AT bus specification, requiring a specific DMA channel.
- PCI/ISA PnP    Devices compliant with the Plug and Play standard, whether designed for PCI or ISA bus architecture.

### PCI/VGA Palette Snoop

Normally this option is always Disabled! Nonstandard VGA display adapters such as overlay cards or MPEG video cards may not show colors properly. Setting Enabled should correct this problem. If this field set Enabled, any I/O access on the ISA bus to the VGA card's palette registers will be reflected on the PCI bus. This will allow overlay cards to adapt to the changing palette colors.

### Assign IRQ For VGA

Many high-end graphics accelerator cards now require an IRQ to function properly. Disabling this feature with such cards will cause improper operation and/or poor performance. Thus, it's best to make sure you enable this feature if you are having problems with your graphics accelerator card. However, some low-end cards don't need an IRQ to run normally. Check your graphics card's documentation (manual). If it states that the card does not require an IRQ, then you can disable this feature to release an IRQ for other uses. When in doubt, it's best to leave it enabled unless you really need the IRQ.

### Assign IRQ For USB

Windows 95 will automatically give an IRQ to the USB port even if there is no USB peripheral connected. Disabling this will free the IRQ.

---

## POST Codes

The following codes are not displayed on the screen. They can only be viewed on the LED display of a so called POST card. The codes are listed in the same order as the according functions are executed at PC startup. If you have access to a POST Card reader, you can watch the system perform each test by the value that's displayed. If the system hangs (if there's a problem) the last value displayed will give you a good idea where and what went wrong, or what's bad on the system board.

CODE	DESCRIPTION OF CHECK
CFh	Test CMOS R/W functionality.
C0h	Early chipset initialization: -Disable shadow RAM -Disable L2 cache (socket 7 or below) -Program basic chipset registers
C1h	Detect memory -Auto-detection of DRAM size, type and ECC. -Auto-detection of L2 cache (socket 7 or below)
C3h	Expand compressed BIOS code to DRAM
C5h	Call chipset hook to copy BIOS back to E000 & F000 shadow RAM.
0h1	Expand the Xgroup codes locating in physical address 1000:0
02h	Reserved
03h	Initial Superio_Early_Init switch.
04h	Reserved
05h	1. Blank out screen 2. Clear CMOS error flag
06h	Reserved
07h	1. Clear 8042 interface 2. Initialize 8042 self-test
08h	1. Test special keyboard controller for Winbond 977 series Super I/O chips. 2. Enable keyboard interface.
09h	Reserved
0Ah	1. Disable PS/2 mouse interface (optional). 2. Auto detect ports for keyboard & mouse followed by a port & interface swap (optional). 3. Reset keyboard for Winbond 977 series Super I/O chips.
0Bh	Reserved
0Ch	Reserved

---

0Dh	Reserved
0Eh	Test F00h segment shadow to see whether it is R/W-able or not. If test fails, keep beeping the speaker.
0Fh	Reserved
10h	Auto detect flash type to load appropriate flash R/W codes into the run time area in F000 for ESCD & DMI support.
11h	Reserved
12h	Use walking 1's algorithm to check out interface in CMOS circuitry. Also set real-time clock power status, and then check for override.
13h	Reserved
14h	Program chipset default values into chipset. Chipset default values are MODBINable by OEM customers.
15h	Reserved
16h	Initial onboard clock generator if Early_Init_Onboard_Generator is defined. See also POST 26h.
17h	Reserved
18h	Detect CPU information including brand, SMI type (Cyrix or Intel) and CPU level (586 or 686).
19h	Reserved
1Ah	Reserved
1Bh	Initial interrupts vector table. If no special specified, all H/W interrupts are directed to SPURIOUS_INT_HDLR & S/W interrupts to SPURIOUS_soft_HDLR.
1Ch	Reserved
1Dh	Initial EARLY_PM_INIT switch.
1Eh	Reserved
1Fh	Load keyboard matrix (notebook platform)
20h	Reserved
21h	HPM initialization (notebook platform)
22h	Reserved
23h	<ol style="list-style-type: none"> <li>1. Check validity of RTC value: e.g. a value of 5Ah is an invalid value for RTC minute.</li> <li>2. Load CMOS settings into BIOS stack. If CMOS checksum fails, use default value instead.</li> </ol>
24h	Prepare BIOS resource map for PCI & PnP use. If ESCD is valid, take into consideration of the ESCD's legacy information.

---

25h	Early PCI Initialization: -Enumerate PCI bus number. -Assign memory & I/O resource -Search for a valid VGA device & VGA BIOS, and put it into C000:0
26h	1. If Early_Init_Onboard_Generator is not defined Onboard clock generator initialization. Disable respective clock resource to empty PCI & DIMM slots. 2. Init onboard PWM 3. Init onboard H/W monitor devices
27h	Initialize INT 09 buffer
28h	Reserved
29h	1. Program CPU internal MTRR (P6 & PII) for 0-640K memory address. 2. Initialize the APIC for Pentium class CPU. 3. Program early chipset according to CMOS setup. Example: onboard IDE controller. 4. Measure CPU speed.
2Ah	Reserved
2Bh	Invoke Video BIOS
2Ch	Reserved
2Dh	1. Initialize double-byte language font (Optional) 2. Put information on screen display, including Award title, CPU type, CPU speed, full screen logo.
2Eh	Reserved
2Fh	Reserved
30h	Reserved
31h	Reserved
32h	Reserved
33h	Reset keyboard if Early_Reset_KB is defined e.g. Winbond 977 series Super I/O chips. See also POST 63h.
34h	Reserved
35h	Test DMA Channel 0
36h	Reserved
37h	Test DMA Channel 1.
38h	Reserved
39h	Test DMA page registers.
3Ah	Reserved
3Bh	Reserved

---

3Ch	Test 8254
3Dh	Reserved
3Eh	Test 8259 interrupt mask bits for channel 1.
3Fh	Reserved
40h	Test 8259 interrupt mask bits for channel 2.
41h	Reserved
42h	Reserved
43h	Test 8259 functionality.
44h	Reserved
45h	Reserved
46h	Reserved
47h	Initialize EISA slot
48h	Reserved
49h	<ol style="list-style-type: none"> <li>1. Calculate total memory by testing the last double word of each 64K page.</li> <li>2. Program write allocation for AMD K5 CPU.</li> </ol>
4Ah	Reserved
4Bh	Reserved
4Ch	Reserved
4Dh	Reserved
4Eh	<ol style="list-style-type: none"> <li>1. Program MTRR of M1 CPU</li> <li>2. Initialize L2 cache for P6 class CPU &amp; program CPU with proper cacheable range.</li> <li>3. Initialize the APIC for P6 class CPU.</li> <li>4. On MP platform, adjust the cacheable range to smaller one in case the cacheable ranges between each CPU are not identical.</li> </ol>
4Fh	Reserved
50h	Initialize USB Keyboard & Mouse.
51h	Reserved
52h	Test all memory (clear all extended memory to 0)
53h	Clear password according to H/W jumper (Optional)
54h	Reserved
55h	Display number of processors (multi-processor platform)
56h	Reserved

---

57h	<ol style="list-style-type: none"> <li>1. Display PnP logo</li> <li>2. Early ISA PnP initialization <ul style="list-style-type: none"> <li>-Assign CSN to every ISA PnP device.</li> </ul> </li> </ol>
58h	Reserved
59h	Initialize the combined Trend Anti-Virus code.
5Ah	Reserved
5Bh	(Optional Feature) Show message for entering AWDFLASH.EXE from FDD (optional)
5Ch	Reserved
5Dh	<ol style="list-style-type: none"> <li>1. Initialize Init_Onboard_Super_IO</li> <li>2. Initialize Init_Onboard_AUDIO.</li> </ol>
5Eh	Reserved
5Fh	Reserved
60h	Okay to enter Setup utility; i.e. not until this POST stage can users enter the CMOS setup utility.
61h	Reserved
62h	Reserved
63h	Reset keyboard if Early_Reset_KB is not defined.
64h	Reserved
65h	Initialize PS/2 Mouse
66h	Reserved
67h	Prepare memory size information for function call: INT 15h ax=E820h
68h	Reserved
69h	Turn on L2 cache
6Ah	Reserved
6Bh	Program chipset registers according to items described in Setup & Auto-configuration table.
6Ch	Reserved
6Dh	<ol style="list-style-type: none"> <li>1. Assign resources to all ISA PnP devices.</li> <li>2. Auto assign ports to onboard COM ports if the corresponding item in Setup is set to "AUTO".</li> </ol>
6Eh	Reserved
6Fh	<ol style="list-style-type: none"> <li>1. Initialize floppy controller</li> <li>2. Set up floppy related fields in 40:hardware.</li> </ol>
70h	Reserved

---

71h	Reserved
72h	Reserved
73h	(Reserved
74h	Reserved
75h	Detect & install all IDE devices: HDD, LS120, ZIP, CDROM.....
76h	(Optional Feature) Enter AWDFLASH.EXE if: -AWDFLASH.EXE is found in floppy drive. -ALT+F2 is pressed.
77h	Detect serial ports & parallel ports.
78h	Reserved
79h	Reserved
7Ah	Detect & install co-processor
7Bh	Reserved
7Ch	Init HDD write protect.
7Dh	Reserved
7Eh	Reserved
7Fh	Switch back to text mode if full screen logo is supported. - If errors occur, report errors & wait for keys - If no errors occur or F1 key is pressed to continue : wClear EPA or customization logo.
80h	Reserved
81h	Reserved

#### E8POST.ASM starts

82h	1. Call chipset power management hook. 2. Recover the text fond used by EPA logo (not for full screen logo) 3. If password is set, ask for password.
83h	Save all data in stack back to CMOS
84h	Initialize ISA PnP boot devices
85h	1. USB final Initialization 2. Switch screen back to text mode
86h	Reserved
87h	NET PC: Build SYSID Structure.
88h	Reserved

---

89h	<ol style="list-style-type: none"> <li>1. Assign IRQs to PCI devices</li> <li>2. Set up ACPI table at top of the memory.</li> </ol>
8Ah	Reserved
8Bh	<ol style="list-style-type: none"> <li>1. Invoke all ISA adapter ROMs</li> <li>2. Invoke all PCI ROMs (except VGA)</li> </ol>
8Ch	Reserved
8Dh	<ol style="list-style-type: none"> <li>1. Enable/Disable Parity Check according to CMOS setup</li> <li>2. APM Initialization</li> </ol>
8Eh	Reserved
8Fh	Clear noise of IRQs
90h	Reserved
91h	Reserved
92h	Reserved
93h	Read HDD boot sector information for Trend Anti-Virus code
94h	<ol style="list-style-type: none"> <li>1. Enable L2 cache</li> <li>2. Program Daylight Saving</li> <li>3. Program boot up speed</li> <li>4. Chipset final initialization.</li> <li>5. Power management final initialization</li> <li>6. Clear screen &amp; display summary table</li> <li>7. Program K6 write allocation</li> <li>8. Program P6 class write combining</li> </ol>
95h	Update keyboard LED & typematic rate
96h	<ol style="list-style-type: none"> <li>1. Build MP table</li> <li>2. Build &amp; update ESCD</li> <li>3. Set CMOS century to 20h or 19h</li> <li>4. Load CMOS time into DOS timer tick</li> <li>5. Build MSIRQ routing table.</li> </ol>
FFh	Boot attempt (INT 19h)

---

## Howto : Flash the BIOS

To flash your BIOS you'll need

- 1) a xxxxx.bin file that is a file image of the new BIOS
- 2) AWDFLASH.EXE a utility that can write the data-file into the BIOS chip.

Create a new, clean DOS 6 bootable floppy with "format a: /s".

Copy flash utility and the BIOS image file to this disk.

Turn your computer off. Insert the floppy you just created and boot the computer. As it boots up, hit the [DEL] key to enter the CMOS setup. Go to "LOAD SETUP (or BIOS) DEFAULTS," and then save and exit the setup program. Continue to boot with the floppy disk.

Type "AWDFLASH" to execute the flash utility. When prompted, enter the name of the new BIOS image and begin the flash procedure. Note: If you reboot now, you may not be able to boot again.

After the flash utility is complete, reboot the system.

### *What to do when the Award flasher says: Insufficient memory*

1. In CMOS Chipset Features Setup, Disable Video Bios Cacheable.
2. Hit Esc, F10, Save and exit.
3. Flash the BIOS and reboot
4. Enter CMOS Chipset Features Setup, and Enable Video Bios Cacheable, hit Esc, F10, Save and reboot.

---

## What if things go wrong

if you use the wrong Flash BIOS or if the writing process gets interrupted, there is a fat chance that your computer won't boot anymore.

### *How can you recover a corrupt BIOS ?*

Boot-block booting (this works only for Award BIOS)

Modern motherboards based on Award BIOS have a boot-block BIOS. This is small area of the BIOS that doesn't get overwritten when you flash a BIOS. The boot-block BIOS only has support for the floppy drive. If you have the AGP video enabled you won't see anything on the screen because the boot-block BIOS only supports an ISA videocard.

If you do not want to change your AGP video setting than proceed as follows:

The boot-block BIOS will execute an AUTOEXEC.BAT file on a bootable diskette. Copy an Award flasher & the correct BIOS \*.bin file on the floppy and execute it automatically by putting awdfash \*.bin in the AUTOEXEC.BAT file.

#### Solution 2: Hot-swapping

1. Replace the corrupt chip by a working one. The working BIOS doesn't have to be written for your board, it just has to give you a chance of booting to DOS.

BIOSs for the same chipset mostly work. (Chipsets that not differ too much also mostly work. (e.g. Triton FX chipset and Triton HX chipset)

2. Boot the system to DOS (with floppy or HD)

3. Be sure that the System BIOS cacheable option in your BIOS is enabled! If so replace (while the computer is powered on) the BIOS chip with the corrupt one. This should work fine with most boards because the BIOS is shadowed in RAM.

4. Flash an appropriate BIOS to the corrupt chip and reboot.

NOTE: Use a flasher from MRBIOS (<http://www.mrbios.com>). Utilities that come with your motherboard often use specific BIOS-hooks. Because you have booted with a BIOS not written for your motherboard they usually don't work. The MR Flash utilities communicate directly with your Flash Rom and always work. In most cases they flash a non-MRBIOS to your BIOS chip without problems.

